MS16550IP

16550 UART Function Compatible IP Module ： Verilog HDL

■ Outline

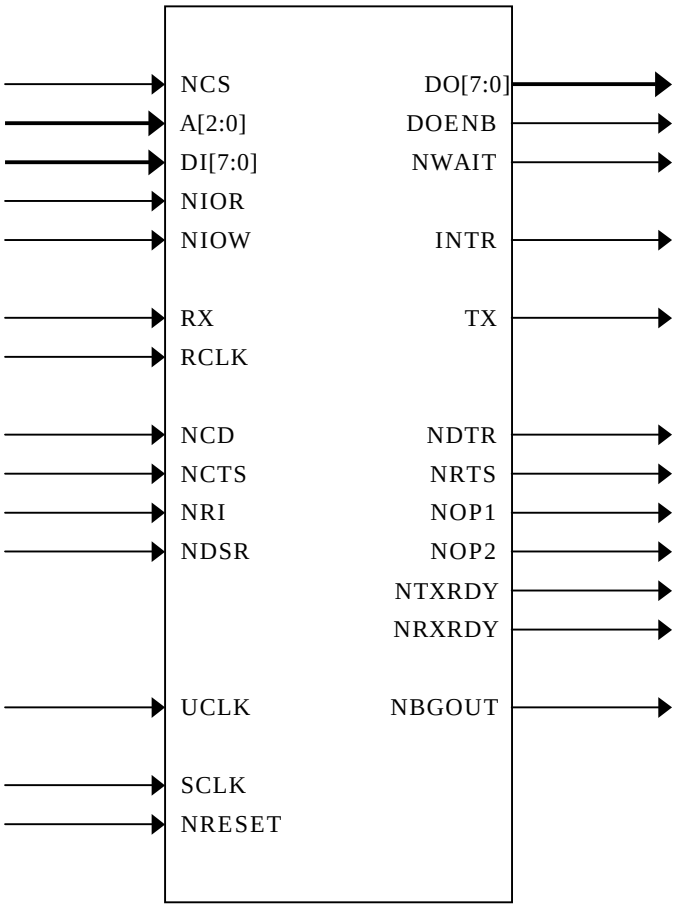
MS16550IP is IP module compatible with 16550UART.

■ Feature

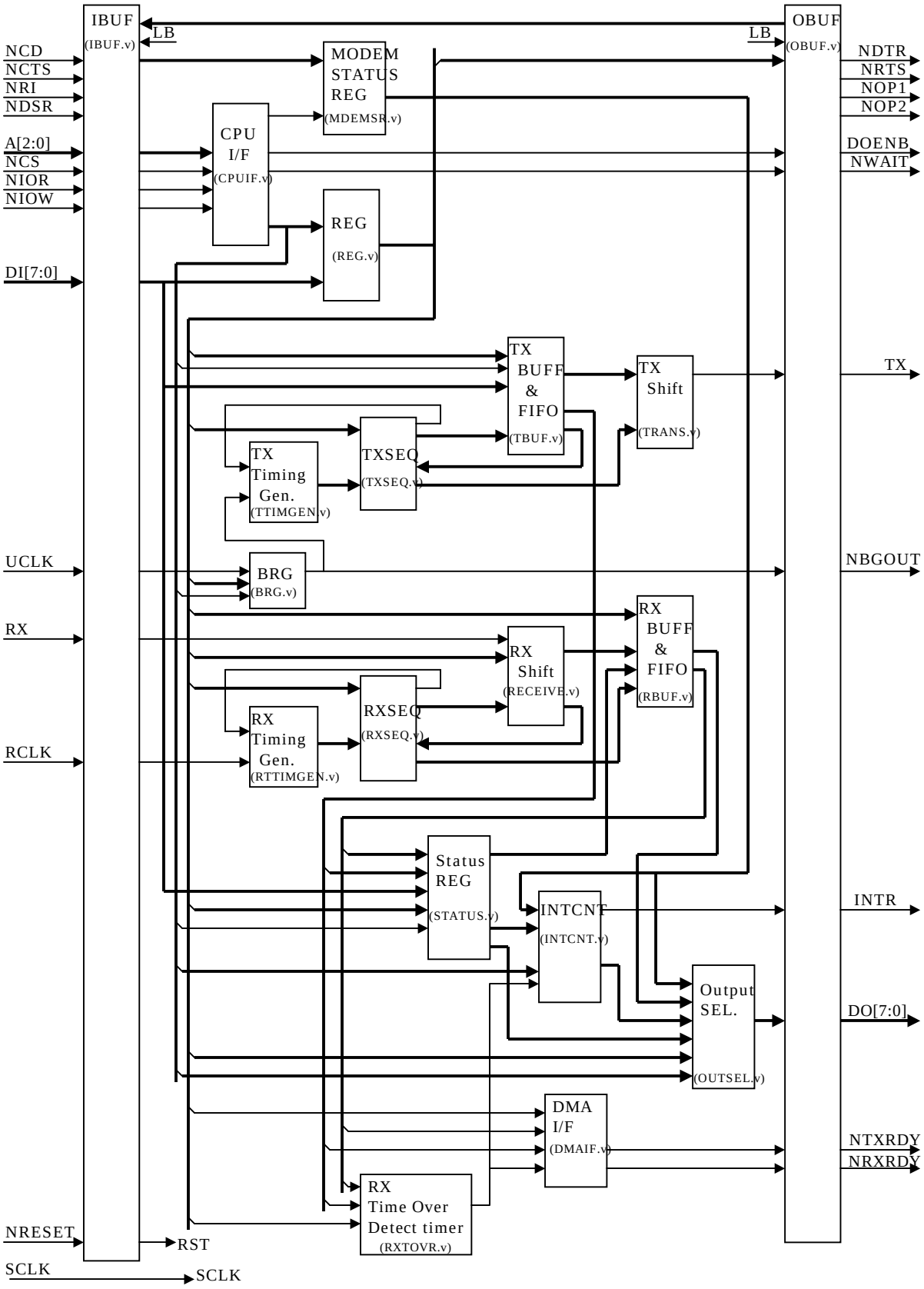
Serial asynchronous receiver data is synchronized and parallel-serial conversion of a transmitter and a receiver is performed.
The synchronization of the serial data adds start/stop bit to the transmission data. The content is guaranteed by adding the parity bit to the data character.
16 bytes are stored in the FIFO in both modes of Rx/Tx. (FIFO mode)
The maximum system efficiency in a minimum system load is obtained.
Four selection level function of the FIFO trigger supplies the maximum data throughput performance, and decreases power consumption.

- ●1.5Mbps Transmitter / Receiver Operation (24Mhz)
- ●16byte transmitter FIFO
- ●16byte receiver FIFO with error flag
- ●Independent transmitter and receiver control
- ●4 Levels for receiver FIFO interrupt trigger level
- ●Standard modem interface
- ●16450 mode supported
- ●Internal synchronization circuit design

■ Input and output signal



■ Block diagram



■ Block explanation

Block name	Function
BRG	Baud rate generator
TX Timing Gen.	Tx timing generation
RX Timing Gen.	Rx timing generation
TX Shift	Tx part ●Tx shift register ●Parity generation ●Output selector
TX BUFF & FIFO	Tx buffer ●16byte FIFO ●Counter for FIFO ●Status generation
TXSEQ	Tx part control
RX Shift	Receiving part ●Start detection ●Rx shift register ●Parity check ●Break detection
RX BUFF & FIFO	Rx buffer ●16*11 bit FIFO ●Counter for FIFO ●Status generation
RX Time Over Detect timer	Rx Time Ovre detect timer
RXSEQ	Rx part control
Status REG	Status register
MODEM STATUS REG	Modem status register
INTCNT	Interrupt controller
REG	Register
CPU I/F	CPU interface
DMA I/F	DMA interface
IBUF OBUF	Input-output buffer and loop back test

■ Input and output signal

Signal name	Polarity	I/O	Timing	Function
NCS	L	I	Asynchronous	Chip select input
A[2:0]	H	I	Asynchronous	Address input
DI[7:0]	H	I	Asynchronous	Data input
NIOR	L	I	Asynchronous	Read strobe input
NIOW	L	I	Asynchronous	Write strobe input
DO[7:0]	H	O	posedge SCLK	Output data
DOENB	H	O	posedge SCLK	Data output enable
NWAIT	L	O	posedge SCLK	Wait demand output
INTR	H	O	posedge SCLK	Interrupt demand output
RX	H	I	Asynchronous	Rx data
RCLK	H	I	Asynchronous	Rx clock input
TX	H	O	posedge SCLK	Tx data
NCD	L	I	Asynchronous	Carrier Detect
NCTS	L	I	Asynchronous	Clear to Send
NRI	L	I	Asynchronous	Ring Indicator
NDSR	L	I	Asynchronous	Data Set Ready
NDTR	L	O	posedge SCLK	Data Terminal Ready
NRTS	L	O	posedge SCLK	Request to Send
NOP1	L	O	posedge SCLK	Output1(User Define)
NOP2	L	O	posedge SCLK	Output2(User Define)
NTXRDY	L	O	posedge SCLK	Transmit Ready
NRXRDY	L	O	posedge SCLK	Receive Ready

UCLK	H	I	Asynchronous	UART standard clock input
NBGOUT	L	O	posedge SCLK	Baud Rate Generator Output
SCLK	H	I	-	System clock input
NRESET	L	I	Asynchronous	System reset input

■ Register explanation

●Register list

Address	DLAB*	R/W	Register Name
0h	Low	W	THR : Transmitter Holding Register
		R	RBR : Receiver Buffer Register
1h	Low	R/W	IER : Interrupt Enable Register
2h	X	W	FCR : FIFO Control Register
		R	ISR : Interrupt Status Register
3h	X	R/W	LCR : Line Control Register
4h	X	R/W	MCR : MODM Control Register
5h	X	R	LSR : Line Status Register
6h	X	R	MSR : MODEM Status Register
7h	X	R/W	SPR : Scratch Pad Register
0h	High	R/W	DLL : Divisor Latch (LSB)
1h	High	R/W	DLM : Divisor Latch (MSB)

* Divisor Latch Read Write permission setting (LCR register)

●Register function

THR / RBR (0h, DLAB=Low)

DB[7:0] : Write -- > Tx data writing (THR)
Read -- > Rx data reading (RBR)

IER (1h, DLAB=Low)

EMSI : Modem status interrupt setting
ELSI : Line status interrupt setting
ETI : Transmitta hold register empty interrupt setting
ERI : Rx data possible interrupt setting

ISR (2h, DLAB=X) Read

FE[1:0] : FIFO Enable check status
IP[2:0] : Interrupt priority check status
IS : Interrupt status check status

FCR (2h, DLAB=X) Write

RT[1:0] : FIFO interrupt trigger level setting
DMS : DMA mode select
XFR : Tx FIFO reset
RFR : Rx FIFO reset
FE : FIFO Enable

LCR (3h, DLAB=X)

DLAB : Divisor Latch Read Write permission setting
SB : Break control setting
SP : Parity bit compulsion set
EPS : Even parity setting
PEN : Parity Enable
STB : Stop bit number specification
WLS[1:0] : Bit number specification of Tx and Rx serial character

MCR (4h, DLAB=X)

LB	:	Local loop back function control for UART self-diagnosis test
OP2	:	User definition NOP2 control
OP1	:	User definition NOP1 control
RTS	:	Request to Send (NRTS) (NDTR) control
DTR	:	Data terminal lady (NDTR) control

LSR (5h, DLAB=X)

FDE	:	FIFO Data Error
TE	:	Transmitter empty indicator
THRE	:	Tx buffer empty indicator
BI	:	Break interrupt indicator
FE	:	Framing error indicator
PE	:	Parity error indicator
OE	:	Overrun error indicator
RDR	:	Receiver data ready indicator

MSR (6h, DLAB=X)

CD	:	Carrier Detect check status
RI	:	Ring Indicator check status
DSR	:	Data Set Ready check status
CTS	:	Clear To Send check status
DCD	:	Carrier detect input (NCD) check status
DRI	:	Ring indicator input (NRI) check status
DDSR	:	Data set ready input (NDSR) check status
DCTS	:	Clear to Send input (NCDTS) check status

SPR (7h, DLAB=X)

D[7:0]	:	Read/Write register of byte

DLL (0h, DLAB=1)

DL[7:0]	:	Low byte side setting register of programmable baud rate generator

DLM (1h, DLAB=1)

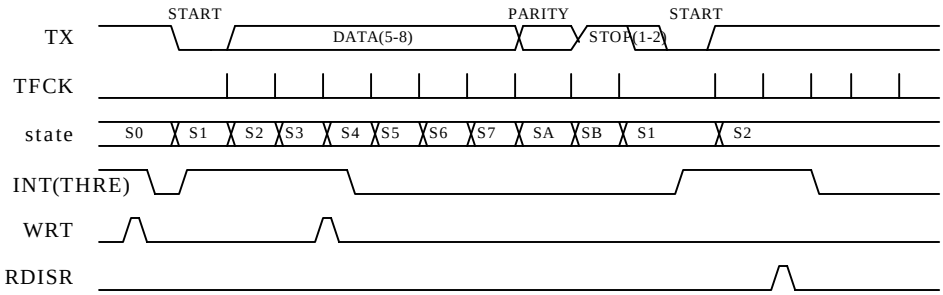
DL[15:8]	:	High byte setting register of programmable baud rate generator

■Tx operation explanation

●16450 Mode

1. Writing data to THR register
2. It is forwarded to the Tx buffer, TFFUL is assert. Tx is started at this time, and the start bit outputs "L".
3. When data is loaded into the shift register, TFEMP is asserted. THRE interrupt is generated . (When Tx hold register/Tx shift register is empty.)
4. Data (TX) is output from the shift register. Sample clock (TFCK) along the setting of data length (WLS) is used.
5. The parity existence is controlled by the LCR-PEN bit, and parity is selected by EPS,SP bit.
6. Tx data outputs "H", and becomes Tx end according to setting (LCR-WLS,STB) of stop bit afterwards. Continuous Tx and TFFUL is assert. In this case, after the stop bit is detected, next data Tx is started.
7. THR Write or ISR Read is needed to clear THRE interrupt.

[Timing diagram]



●16550 Mode

Because it has the FIFO in 16*8 bits, the set condition of TFEMP and TFFUL is different from 16450 modes.

If data doesn't exist in the Tx buffer at all, TFEMP is assert. And, when data is preserved in all 16 bytes FIFOs, TFFUL

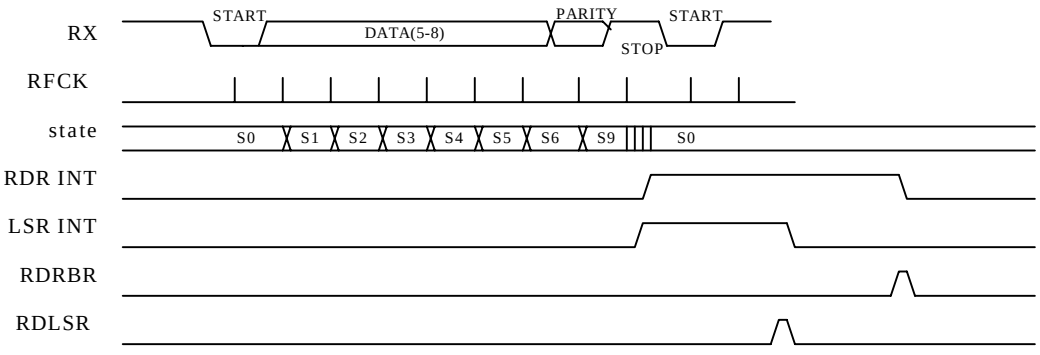
is assert.

■Rx operation explanation

●16450 Mode

1. The internal receiver counter begins to count by 16 times the clock rate starting with the negative edge of the start signal. The purpose of it is "Mis-start detection" prevention. If did the hold of "L" by eight clocks, it detects it as a start bit. It synchronizes again when "H" is detected on the way. Receive data is shifted at the center of data.
2. Sample clock (RFCK) receives the data at the center of each data according to "LCR-WLS setting".
3. If the LCR-PEN bit is "H", it is a parity bit. It judges whether the parity bit is corresponding to "Parity selection (LCR-EPS,SP)". After the Rx ends, parity error (PE) is output when neither the parity bit nor the parity selection are corresponding.
4. If the stop bit is "H", then Rx end and RFFUL are asserted. Receive data ready interruption (RDR) is generated. The condition of Framing error (FE) generation is a stop bit "L". If it is Break Rx (RXBRK), Break interrupt (BI).
5. The RBR Read is necessary to clear the RDR interruption. The LSR Read is necessary to clear OE, PE, FE, and the BI interruption.

[Timing chart]



●16550 Mode

Because it has the FIFO in 16*11 bits, the set condition of RFFUL and RFEMP and the set conditions of error (PE,FE,BI) are different from 16450 modes.

RFEMP when data doesn't exist in the Rx buffer FIFO at all is assert . RFFUL when there is all data in the FIFO is assert. Error indication shows the content of the data of the part that the pointer of the FIFO has marked.

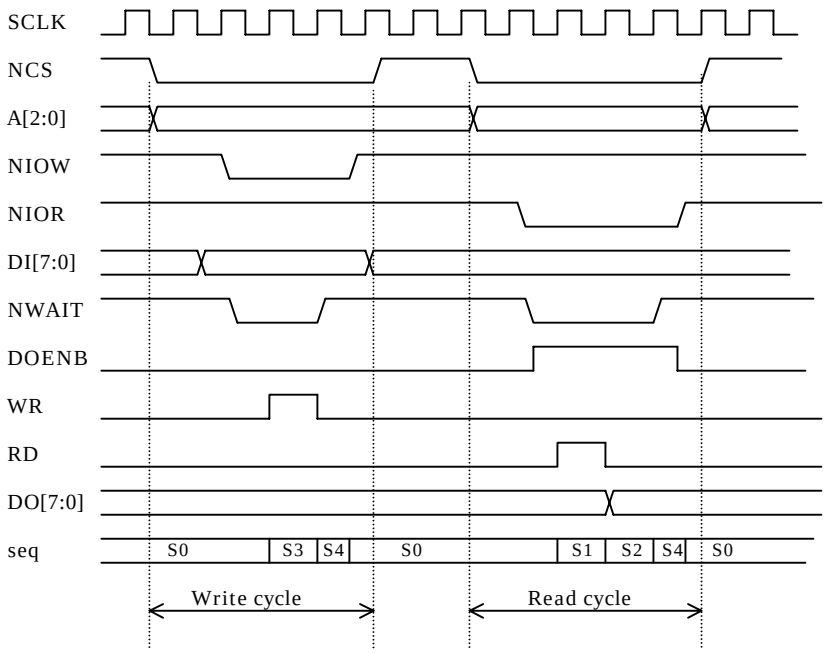
Error clear by LSR Read. The pointer is renewed to Next FIFO by the RBR Read.

In "16550 modes", the trigger level setting can be done. The RFTL interrupt is generated when becoming more than the

trigger level to which it is set.

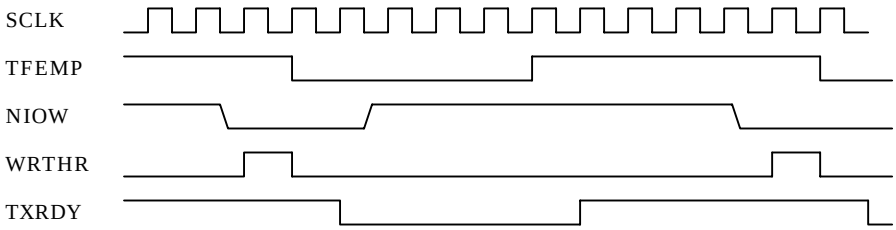
■CPU access timing

This IP is gesigned for PCMCIA I/O. When the system clock or the target interface are different, the module change is necessary. We do changing by your reqest.

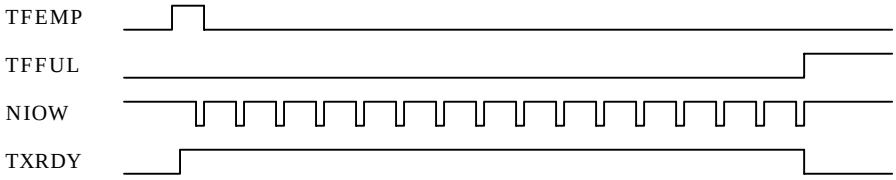


■DMA transfer (TXRDY and RXRDY signal)

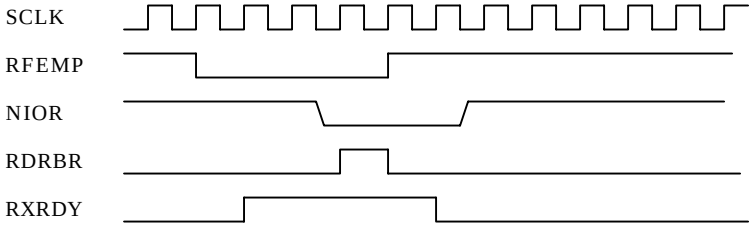
TXRDY : At DMA transfer mode 0(DMS=0: starting value)



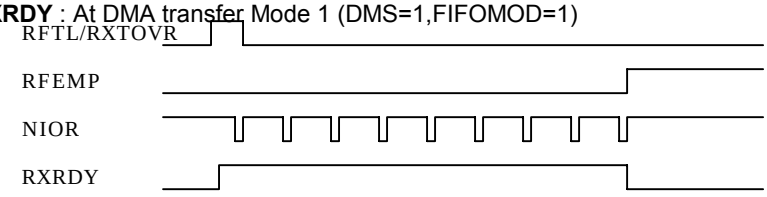
TXRDY : At DMA transfer Mode 1 (DMS=1,FIFOMOD=1)



RXRDY : At DMA transfer mode 0(DMS=0: starting value)



RXRDY : At DMA transfer Mode 1 (DMS=1,FIFOMOD=1)



1 . This data sheet may be changed without any notification for improvement.

2. We have no responsibility that this product may infringe any right.

3. No part of this document may be reproduced in any form without the prior written consent of us.