MS40302

CMOS I2S SOUND DATA DELAY LINE LSI

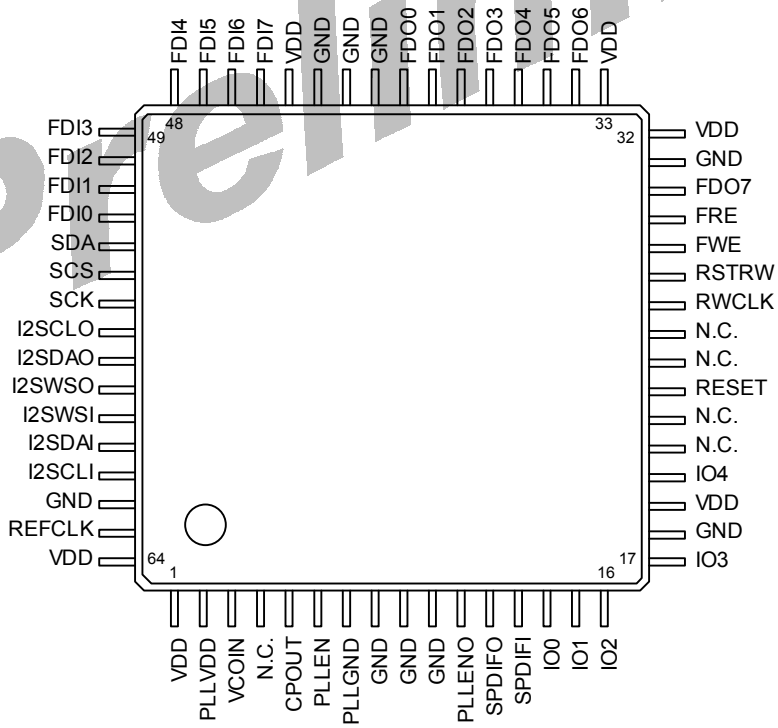
■ Outline

This LSI is "Sound data delay LSI" which carries out delay output of "Sound data input based on the I2S bus interface".

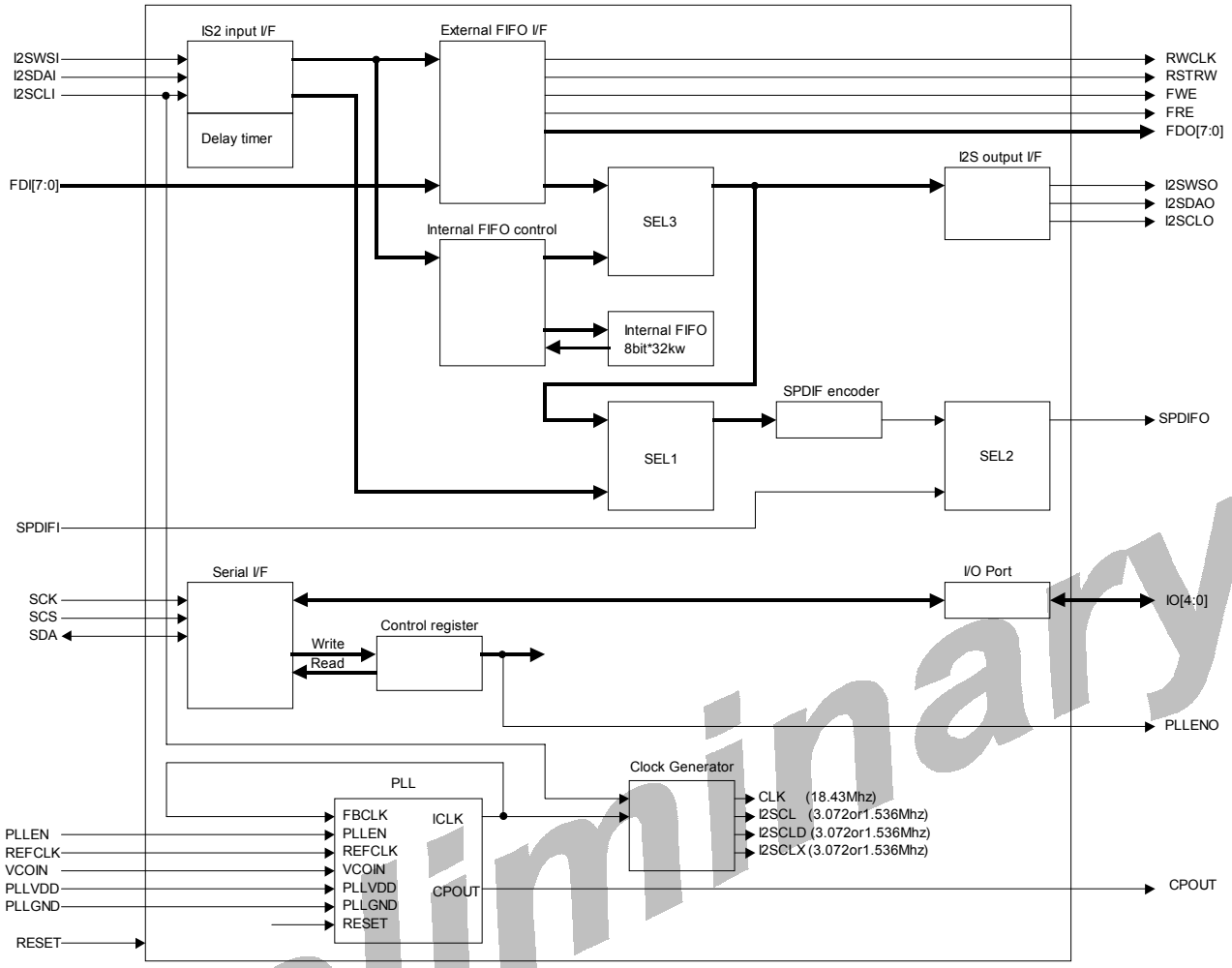
■ Feature

- Sound input format : I2S (three lines) format.
- Sound output format: I2S (three lines) format, S/PDIF format.
- Available below three kind I2S format.
  1) 16bit_data / 16bit_format , 2) 16bit_data / 32bit_format , 3) 24bit_data / 32bit_format
- Sound data delay time is programmable.
- FIFO for Sound data delay is SRAM of 256Kbit (External FIFO is connectable up to 2Mbit).
- S/PDIF format output is chosen from three kinds of Sound data.
  1) Delay I2S data, 2) No delay I2S data, 3) S/PDIF input through
- Can be used as data format conversion (I2S -> S/PDIF) IC.
- 2's compliment conversion function for S/PDIF encoder is attached.
- PLL is equipped.
- 3 line serial control based on Tbus2 standard.
- 5bit extension I/O Port is equipped.
- LQFP-64pin

■ Package



■ Block diagram



■ Input and output signal

Grouping	Signal name	I/O	Polarity	Description
I2S I/F	I2SWSI	I	5V tolerant input	I2SWS input (48KHz L : LchData , H : RchData)
	I2SDAI	I	5V tolerant input	I2SDA input
	I2SCLI	I	5V tolerant input	I2SCL input (32bitMode : 3.072MHz , 16bitMode : 1.536MHz)
	I2SWSO	O		I2SWS output (48KHzL : LchData , H : RchData)
	I2SDAO	O		I2SDA output
	I2SCLO	O		I2SCL output (32bitMode : 3.072MHz , 16bitMode : 1.536MHz)
S/PDIF	SPDIFI	I	5V tolerant input	S/PDIF input (3.072Mbps)
	SPDIFO	O		S/PDIF output (3.072Mbps)
Serial I/F	SCK	I	5V tolerant, Schmitt Trigger input	Serial communication clock (Tbus2 Clock)
	SCS	I	5V tolerant, Schmitt Trigger input	Serial communication chip select (Tbus2 Period)
	SDA	I/O	5V tolerant, Schmitt Trigger input	Serial communication data (Tbus2 Data)
	PLLENO	O		PLL enable setting output (Connects to PLLEN input)
PLL	PLLEN	I		PLL enable (Connects to PLLENO)
	REFCLK	I	5V tolerant input	PLL reference clock input (Connects with I2SCLI externally)
	CPOUT	O		Charge Pump Out (Constitutes loop filter externally)
	VCOIN	I		VCOIn(Constitutes loop filter externally)
FIFO	FDO[7:0]	O		Extended FIFO data output
	FDI[7:0]	I	Pull Up	Extended FIFO data input
	RWCLK	O		Extended FIFO R/W clock (18MHz)
	FWE	O	"H" active	Extended FIFO Write enable
	FRE	O	"H" active	Extended FIFO Read enable
	RSTRW	O	"H" active	Extended FIFO Master reset
PORT	IO[4:0]	I/O	Pull Up, 5V tolerant input	Extension I/O
Global	RESET	I	"L" active, 5V tolerant input	Asynchronous reset input
PLL power supply	PLLVDD	-		VDD(3.3V) power supply for PLL
	PLLGND	-		GND(0V)
power supply	VDD	-		VDD(3.3V)
	GND	-		GND(0V)

■ Electrical definition

● Absolute maximum rating (Vss=0V)

Parameter	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.3 ~ 4.0	V
Input voltage	V_{IN}	-0.3~ V_{DD} + 0.5	V
Output current	I_{OUT}	± 3.0	V
Storage Temperature	T_{STG}	- 55 ~ +125	° C

● Recommended operating condition（Vss=0V）

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating Temperature	Topr	- 40	-	85	°C

● D.C. characteristics

TBD

■ Register MAP

Device address = 0ch (LSB First)

Sub address	Register name								
00h	MODE setting	7	6	5	4	3	2	1	0
		-	-	-	SEL3	SEL2	SEL1	MODE[1]	MODE[0]
		R(0)	R(0)	R(0)	R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(0)
01h	DELAY setting	7	6	5	4	3	2	1	0
		DELAY[7]	DELAY[6]	DELAY[5]	DELAY[4]	DELAY[3]	DELAY[2]	DELAY[1]	DELAY[0]
		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)
02h	SPDIF setting	7	6	5	4	3	2	1	0
		CISET2	FSSET[1]	FSSET[0]	NUM	VSET	CSET	CISET	CHSET
		R/W(0)	R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(0)
03h	Control of operation	7	6	5	4	3	2	1	0
		-	-	-	-	FINIT	I2SGO	DEVRDY	PLLEN
		R(0)	R(0)	R(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)
04h	Port setting	7	6	5	4	3	2	1	0
		-	-	-	IO4	IO3	IO2	IO1	IO0
		R(0)	R(0)	R(0)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
05h	Port output	7	6	5	4	3	2	1	0
		-	-	-	DO4	DO3	DO2	DO1	DO0
		R(0)	R(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)
06h	Port input	7	6	5	4	3	2	1	0
		-	-	-	DI4	DI3	DI2	DI1	DI0
		R(0)	R(0)	R(0)	R(x)	R(x)	R(x)	R(x)	R(x)

■ Register function

MODE setting (00h)

MODE[1:0] : I2S mode setting
SEL1 : S/PDIF decoding select
SEL2 : S/PDIF output select
SEL3 : FIFO select

DELAY setting (01h)

DELAY[7:0] : DELAY value setting

SPDIF setting (02h)

CHSET : Channel status setting
CISET2 , CISET : Copyright information setting
CSET : Copyright Protection setting
VSET : S/PDIF format V value setting
NUM : I2S -> S/PDIF data conversion
FSSET[1:0] : Sampling frequency setting

Control of operation (03h)

PLLEN : PLL operation start
DEVRDY : Device Ready
I2SGO : I2S delay operation start
FINIT : External FIFO initialization start trigger

Port setting (04h)

IO[4:0] : Extended I/O input and output setting

Port output (05h)

DO[4:0] : Extended I/O output setting

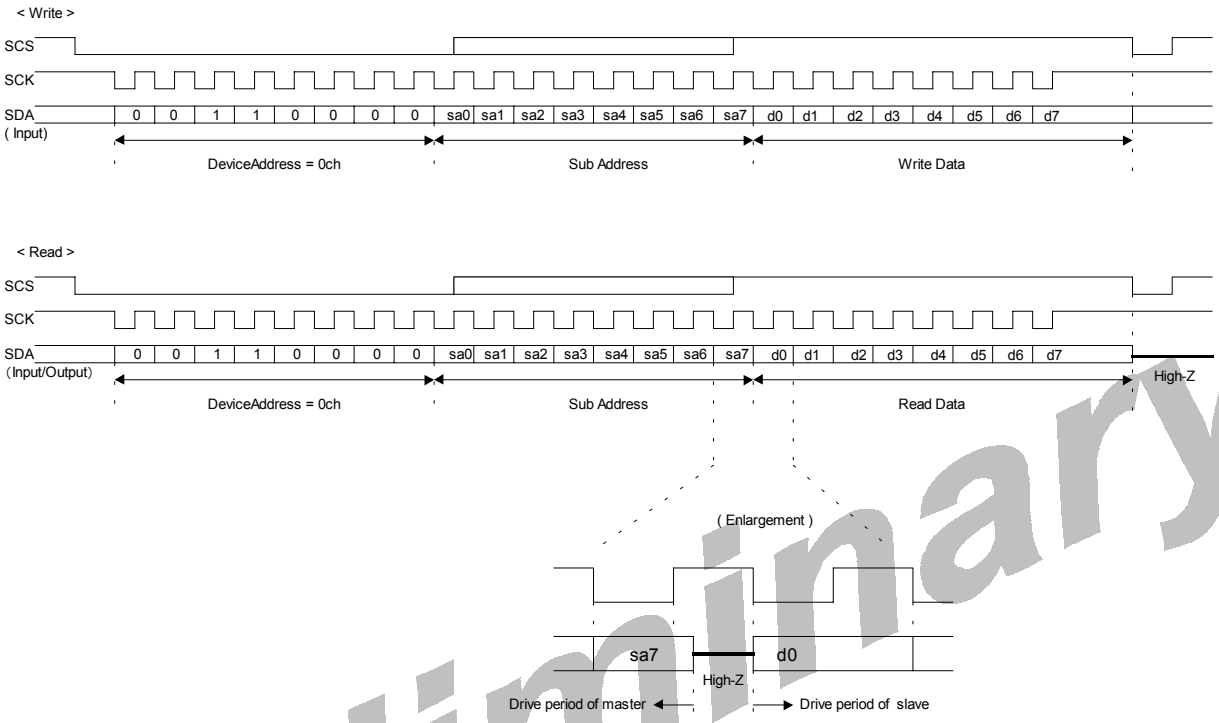
Port input (06h)

DI[4:0] : Extended I/O input setting

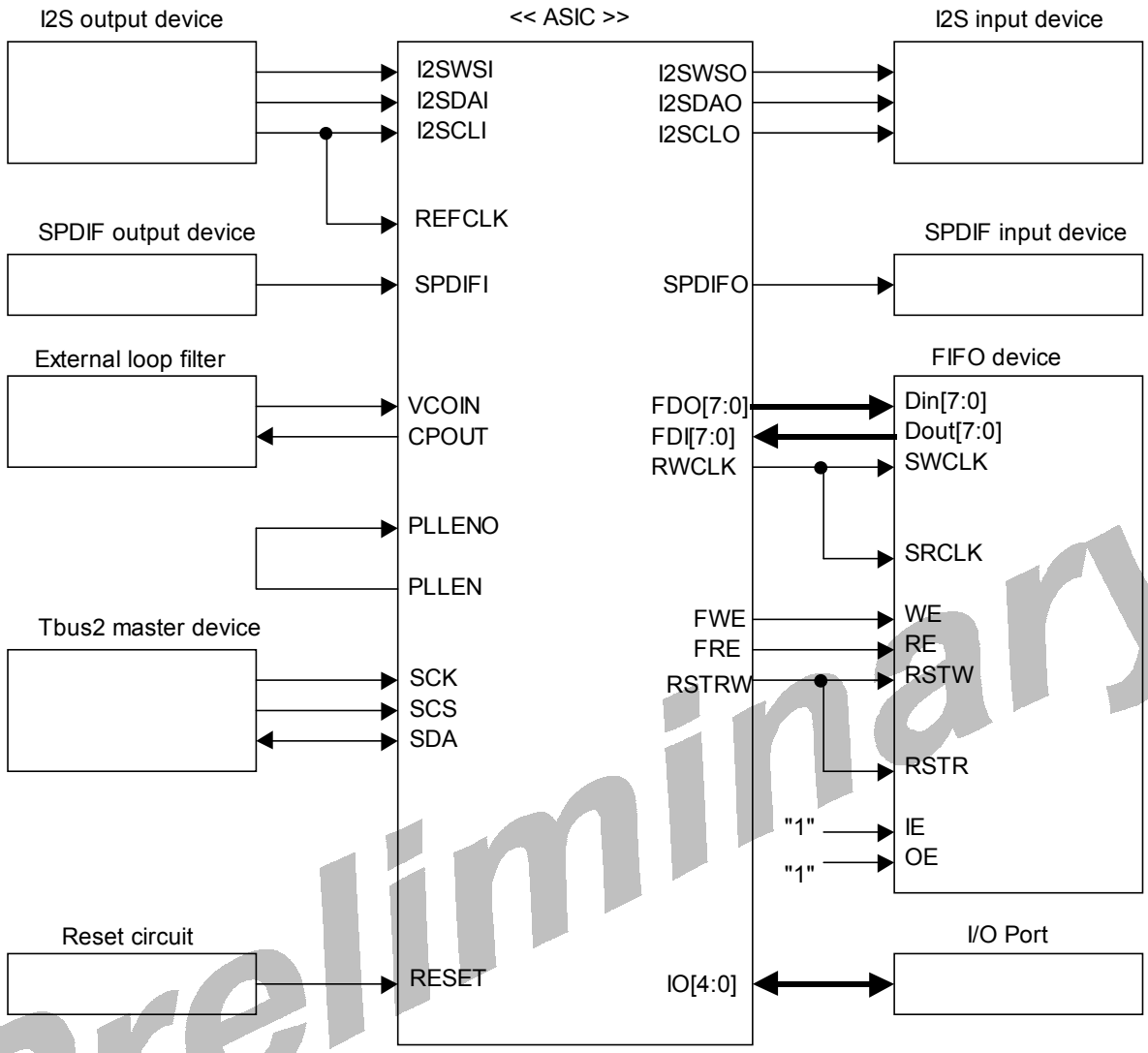
■ Serial interface

3 line serial control interface based on tbus2 standard. It operates as slave of basic composition.

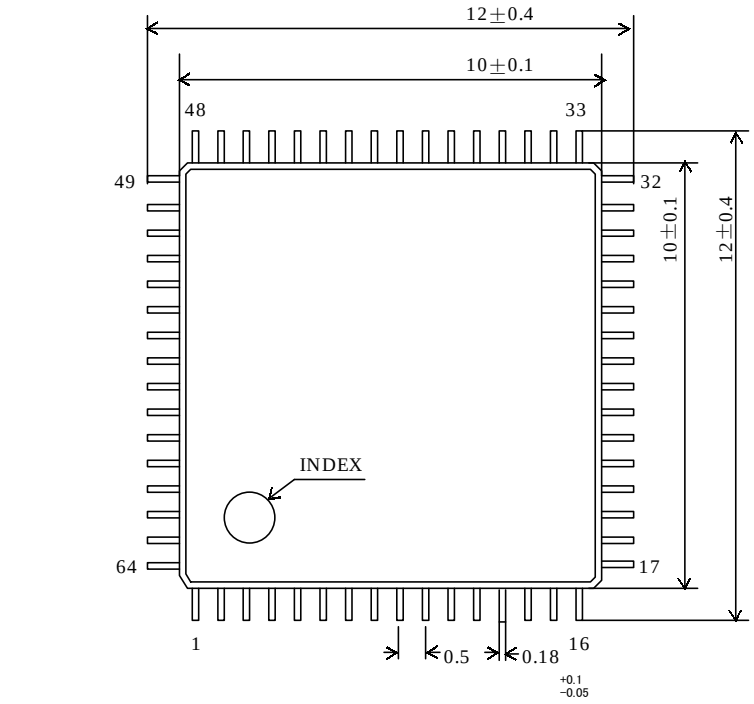
Device address : 0ch
Sub-address : 8bit register is assigned on 00h-06h.
Reset address : 00h. All circuits(include register) except serial control circuit are reset internally.

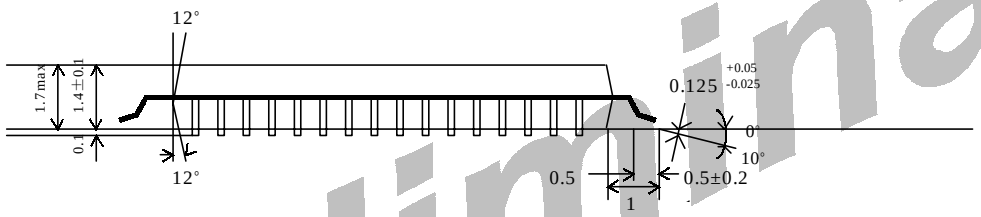


■ Example of peripheral circuit connection



■ Package size





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