MS40402

CMOS I2S SPDIF AUDIO DATA DELAY LINE LSI

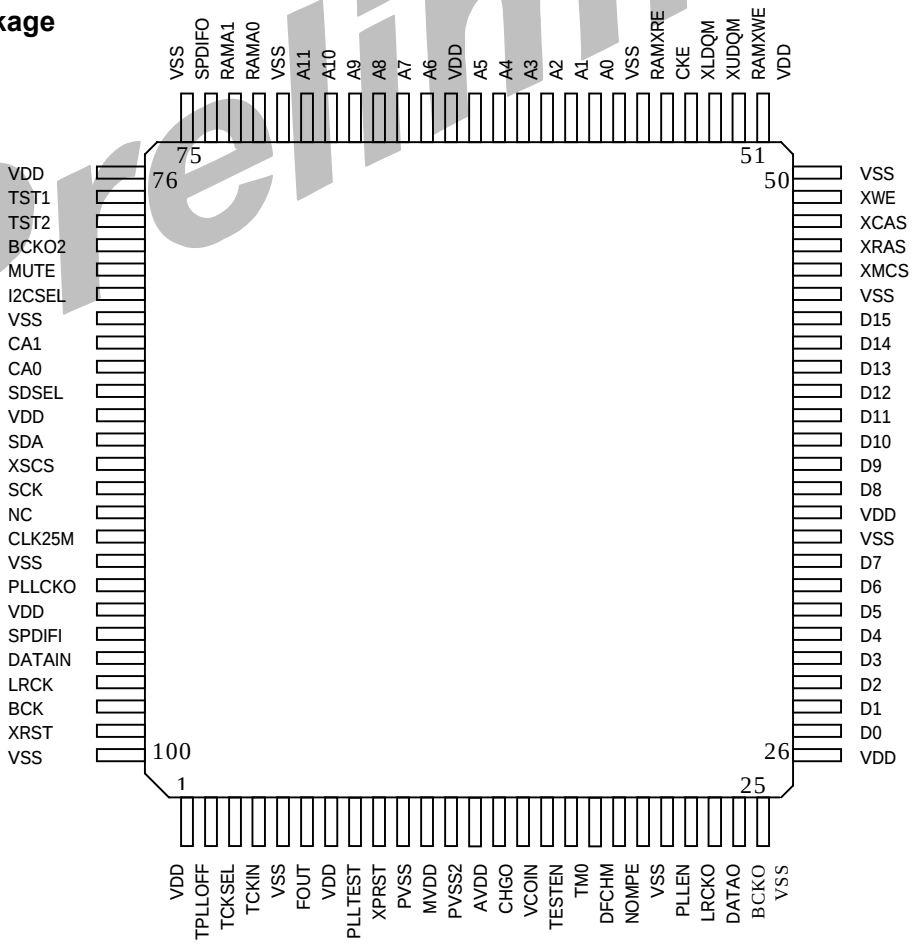
■ Outline

This LSI is "Sound data delay LSI" which carries out delay output of "Sound data input based on the I2S and S/PDIF bus interface ".

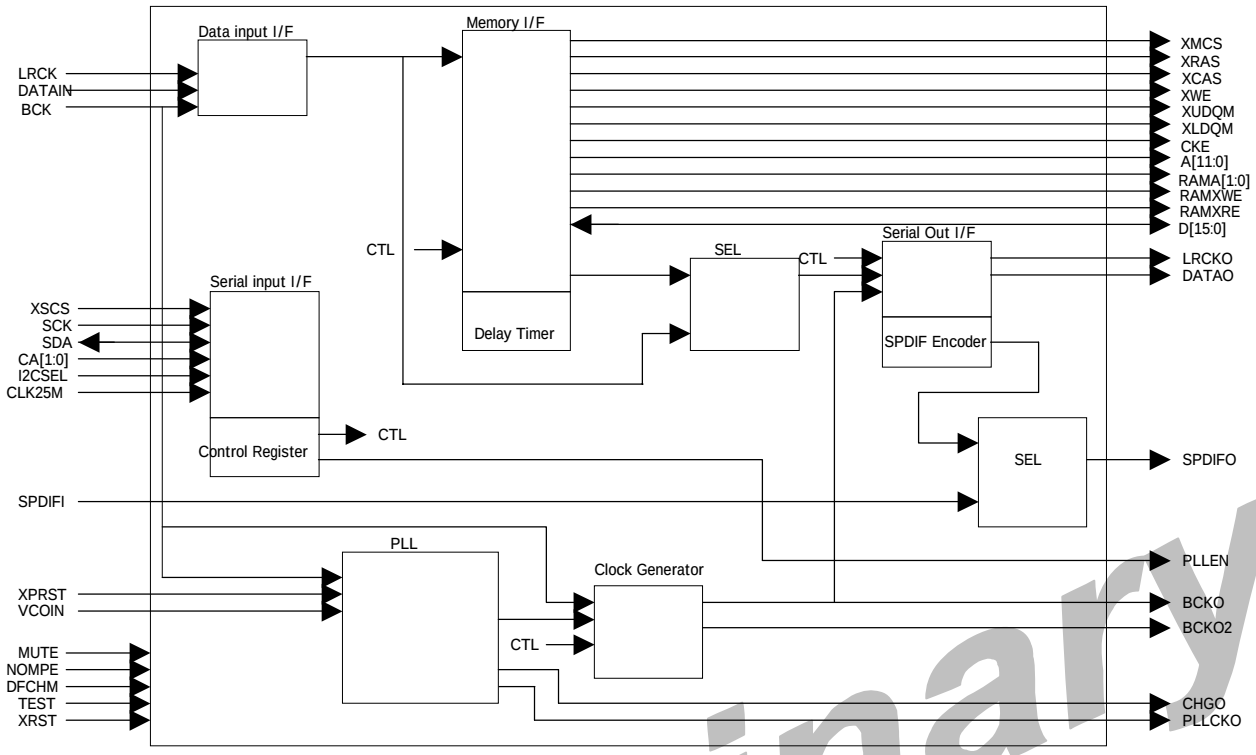
■ Feature

- Sound input format : I2S (3 lines) format, S/PDIF format.
- Sound output format: I2S (3 lines) format, S/PDIF format.
- Available below three kind I2S format.
  1) 16bit_data / 16bit_format , 2) 16bit_data / 32bit_format , 3) 24bit_data / 32bit_format
- Sound data delay time is programmable.
- FIFO for Sound data delay is External SDRAM or SRAM up to 16Mbit.
- S/PDIF format output is selected by register setting.
  1) Delayed sound data, 2) S/PDIF input data through
- Can be used as data format conversion (I2S -> S/PDIF) or (S/PDIF -> I2S) IC.
- Maximum delay time is about 8 sec.(at 32KHz Sampling) 1.36 sec.(at 192KHz Sampling).
- Unit delay time is 6 msec.(at 32KHz Sampling) 1 msec.(at 192KHz Sampling).
- PLL is built-in.
- 3 line serial control or I2C bus serial control.
- LQFP-100pin

■ Package



■ Block diagram



■ Input and output signal

Grouping	Signal name	I/O	Polarity etc.	Description
Audio I/F	LRCK	I		LRCK input (Sampling Freq.32 to 192KHz, Lch, Rch Data assigning signal)
	DATAIN	I		Audio Data input (I2S or S/PDIF format)
	BCK	I		Bit Clock input (32KHz I2S: 1.024MHz, 192KHz S/PDIF: 24.576MHz)
	LRCKO	O		LRCK output (Sampling Freq.32 to 192KHz, Lch, Rch Data assigning signal)
	DATAO	O		Audio Data output (I2S,S/PDIF format)
	BCKO	O		Bit Clock output (32KHz I2S: 1.024MHz, 192KHz S/PDIF: 24.576MHz)
	BCKO2	O		Bit Clock output2 (Relating with SPDIFO)
S/PDIF	SPDIFI	I		S/PDIF input (2.048Mbps to 12.288Mbps)
	SPDIFO	O		S/PDIF output (2.048Mbps to 12.288Mbps)
Serial I/F	SCK	I	High Active	Serial interface clock
	XSCS	I	Low Active	Serial interface chip select (High forced at I2C Mode)
	SDA	I/O		Serial interface data
	CLK25M	I		10 to 25MHz clock input (necessary at I2C mode only)
	I2CSEL	I		I2C mode select for serial interface
	CA[1:0]	I		Device address input for serial interface
PLL	XPRST	I	Low Active	PLL reset (Connect to PLLEN)
	FOUT	O		PLL Clock output monitor
	PLLCKO	O		PLL Clock output monitor (1/4 PLL clock Freq.)
	CHGO	O		Charge Pump Out (Connect to external loop filter)
	VCOIN	I		VCOIN (Connect to external loop filter)
Memory	D[15:0]	I/O		External Memory(SDRAM or SRAM) data bus
	A[11:0]	O		External Memory(SDRAM or SRAM) address bus
	RAMXWE	O	Low Active	External SRAM Write enable
	XWE	O	Low Active	External SDRAM Write enable (SRAM A15)
	XRAS	O	Low Active	External SDRAM RAS (SRAM A17)
	XCAS	O	Low Active	External SDRAM CAS (SRAM A16)
	XUDQM	O	Low Active	External SDRAM UDQM (SRAM A14)
	XLDQM	O	Low Active	External SDRAM LDQM (SRAM A13)
	CKE	O	High Active	External SDRAM CKE (SRAM A12)
	RAMXRE	O	Low Active	External SRAM Read enable
	XMCS	O	Low Active	External Memory (SDRAM,SRAM) Chip select
	RAMA[1:0]	O		External SRAM address (A18,19)
Control	SDSEL	I		External Memory select (High:SDRAM,Low:SRAM)
	NOMPE	I	With Pull down R	Output control at Parity Error occurred
	DFCHM	I	With Pull down R	Data format change mode
	MUTE	I		Audio Output data muting
	PLLEN	O		PLL enable output
Global	XRST	I	Low active	Asynchronous reset input
PLL power supply	MVDD	-		VDD(3.3V) power supply for PLL
	PVSS	-		GND(0V) power supply for PLL
	PVSS2	-		GND(0V) power supply for PLL low pass filter
	AVDD	-		VDD(3.3V) power supply for PLL low pass filter
power supply	VDD	-		VDD(3.3V)
	VSS	-		GND(0V)

■ Electrical definition

● Absolute maximum rating (Vss=0V)

Parameter	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.3 ~ 4.0	V
Input voltage	V_{IN}	-0.3~ V_{DD} + 0.5	V
Output current	I_{OUT}	± 3.0	V
Storage Temperature	T_{STG}	- 55 ~ +125	° C

● Recommended operating condition (Vss=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating Temperature	Topr	- 40	-	85	°C

● D.C. characteristics

TBD

■ Register MAP

Device address ={CA1,CA0},(MSB First) : for 3line serial control
={1000,CA1,CA0}(MSB First) :for I2C

Sub address	Register name								
00h	MODE setting	7	6	5	4	3	2	1	0
		SEL	-	-	-	OUTSEL1	OUTSEL0	INPSEL1	INPSEL0
		R/W(0)	R(0)	R(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)
01h	DELAY setting	7	6	5	4	3	2	1	0
		DELAY[7]	DELAY[6]	DELAY[5]	DELAY[4]	DELAY[3]	DELAY[2]	DELAY[1]	DELAY[0]
		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)
02h	DEALY setting	7	6	5	4	3	2	1	0
		-	-	-	-	-	DELAY[10]	DELAY[9]	DELAY[8]
		R(0)	R(0)	R(0)	R(0)	R(0)	R/W(0)	R/W(0)	R/W(0)
03h	SPDIF setting	7	6	5	4	3	2	1	0
		FSSET2	FSSET1	FSSET0	VSET	CSET	CLSET	CISET	CHSET
		R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)
04h	Control setting	7	6	5	4	3	2	1	0
		PERRCLR	-	FMUTE	MUTE	MINIT	DLYSTA	DVRDY	PLLEN
		R/W(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)
05h	Error	7	6	5	4	3	2	1	0
		-	-	-	-	-	-	-	PERR
		R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)	R(0)

■ Register function

MODE setting (00h)

SEL : SPDIFO output select
OUTSEL[1:0] : Output data format select
INPSEL[1:0] : Input data format select

DELAY setting (01h)

DELAY[7:0] : DELAY value setting lower

DELAY setting (02h)

DELAY[10:8] : DELAY value setting upper

SPDIF setting (03h)

CHSET : Channel status setting
CISET , CISET : Copyright information setting
CSET : Copyright Protection setting
VSET : S/PDIF format V value setting
FSSET[2:0] : Sampling frequency setting

CONTROL setting (04h)

PLLEN : PLL operation start
DEVRDY : Device Ready
DLYSTA : Delay operation start
MINT : External SDRAM initialization start trigger
MUTE : Muting output data
FMUTE Muting output data
PERRCLR : Parity error clear

ERROR register (05h)

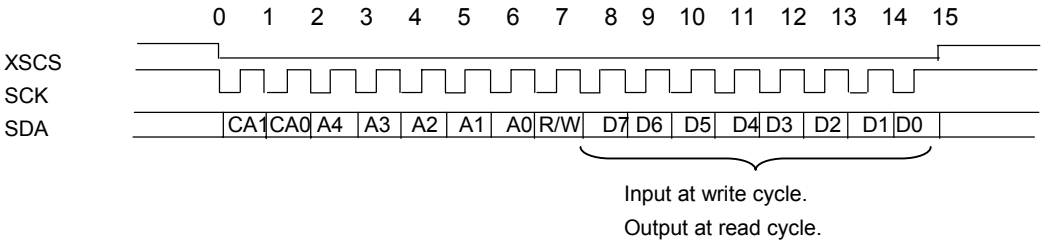
PERR : Parity error occur

■ Serial interface

●3 line serial control interface. (I2CSEL=Low)

Device address : {CA1,CA0}

Sub-address : 5bit register is assigned on 00h-05h.



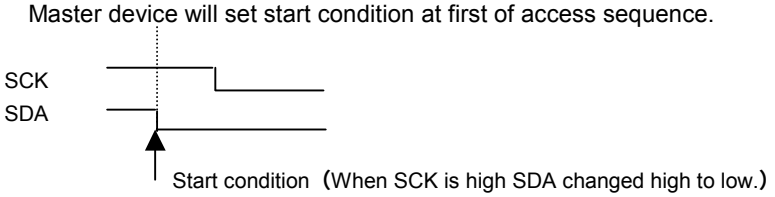
* Data is imported at positive edge of SCK and internal register data is set at positive edge of XSCS.

●I2C serial control interface. (I2CSEL=High)

This IC is operating as slave mode device of I2C bus.

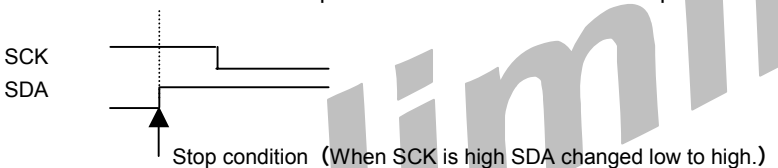
1. Start condition

   Master device will set start condition at first of access sequence.

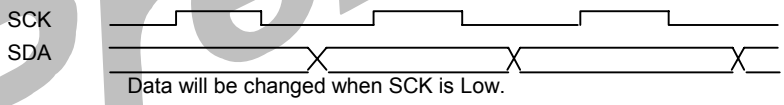


2. Stop condition

   Master device will set stop condition at end of access sequence.



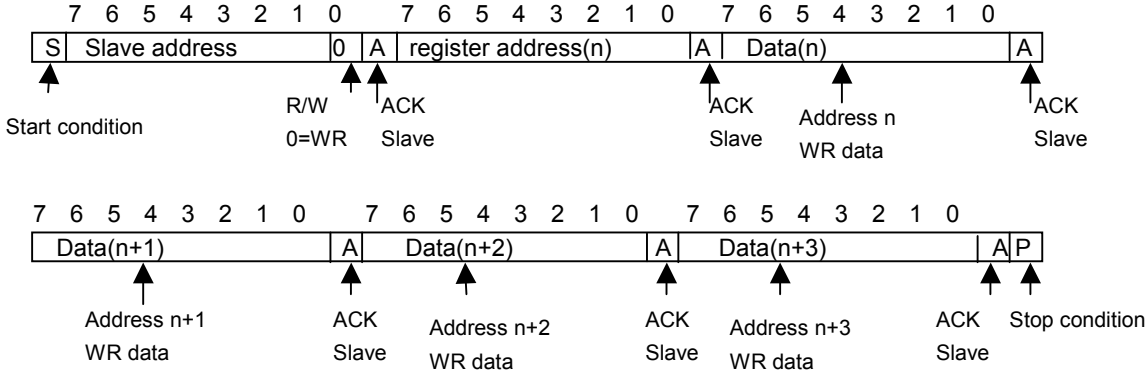
3. Data transfer



4. Acknowledge generation

   This device will generate acknowledge after 1byte data transfer has completed from master device.
   Acknowledge (ACK) is that this device assert SDA to low level.

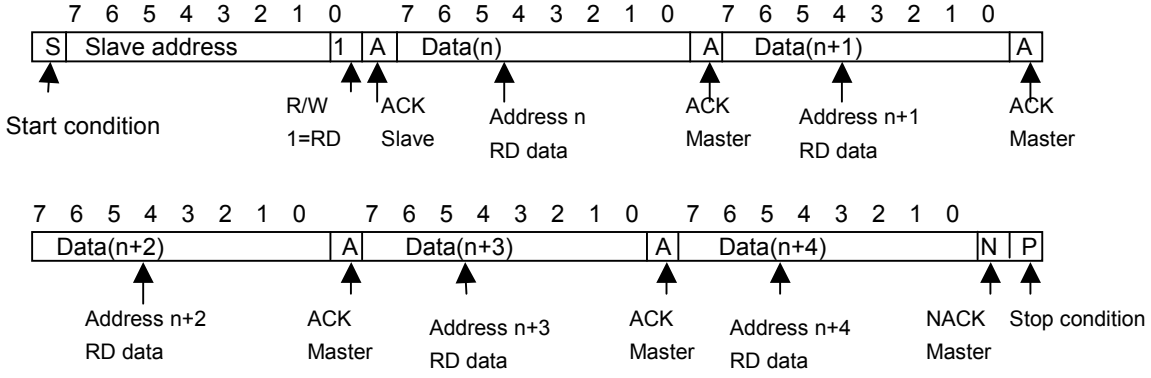
5. Data write cycle



*Slave address=10000,CA1,CA0 (CA1,CA0 **are input terminals setting)**

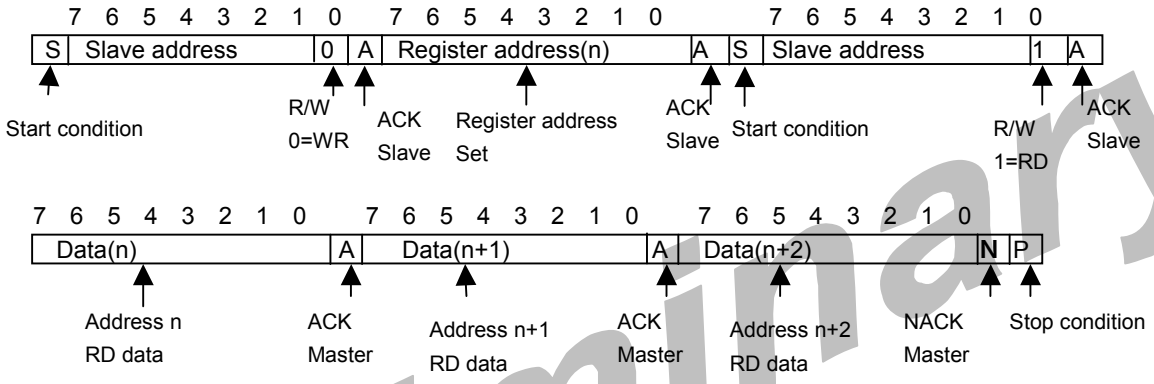
*You should set register address with 8bit format.

6. Current address read



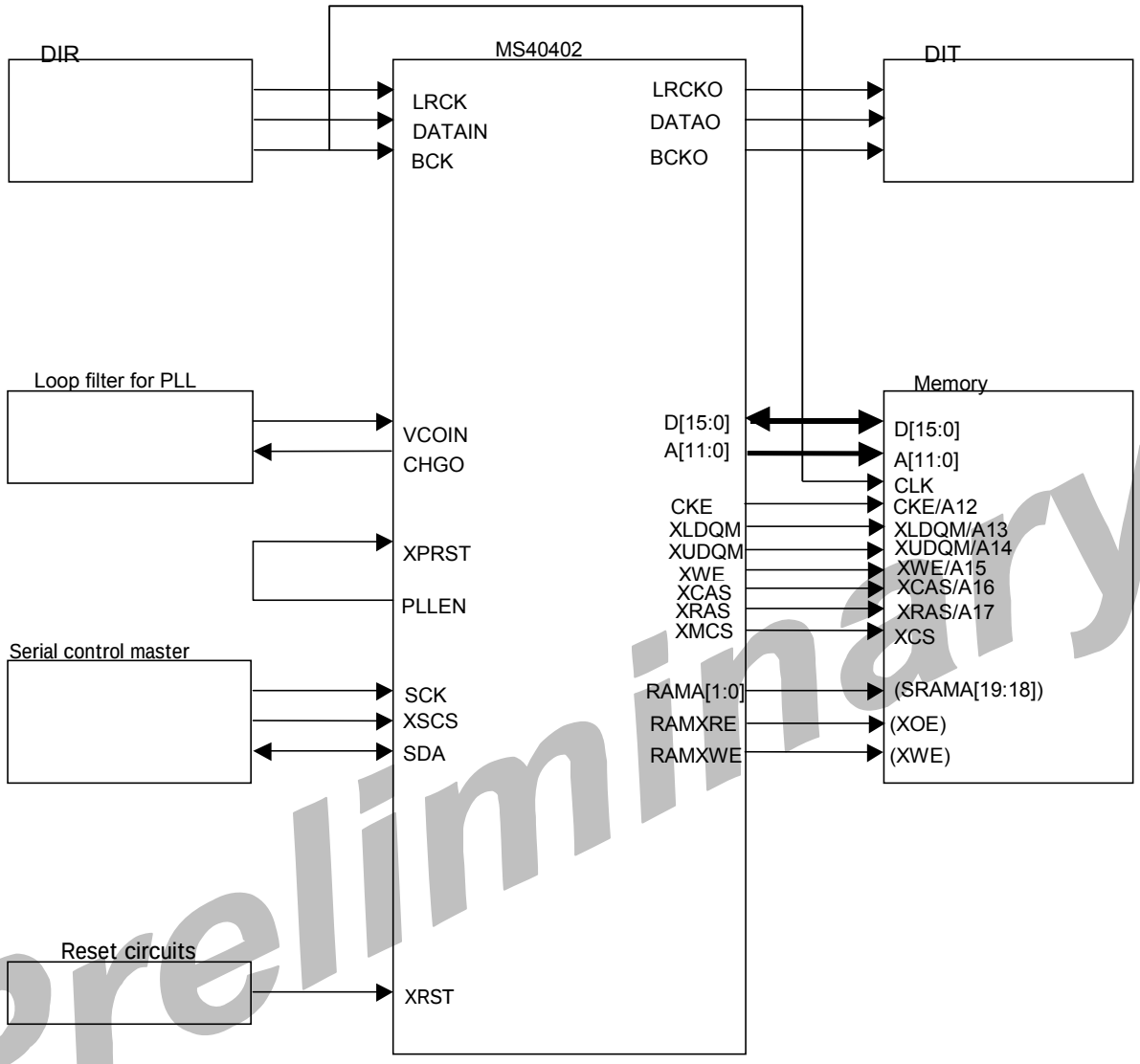
*Slave address=10000,CA1,CA0 (CA1,CA0 **are input terminals setting**)
*Data read is performed incremental based from former register access address.

7. Random read

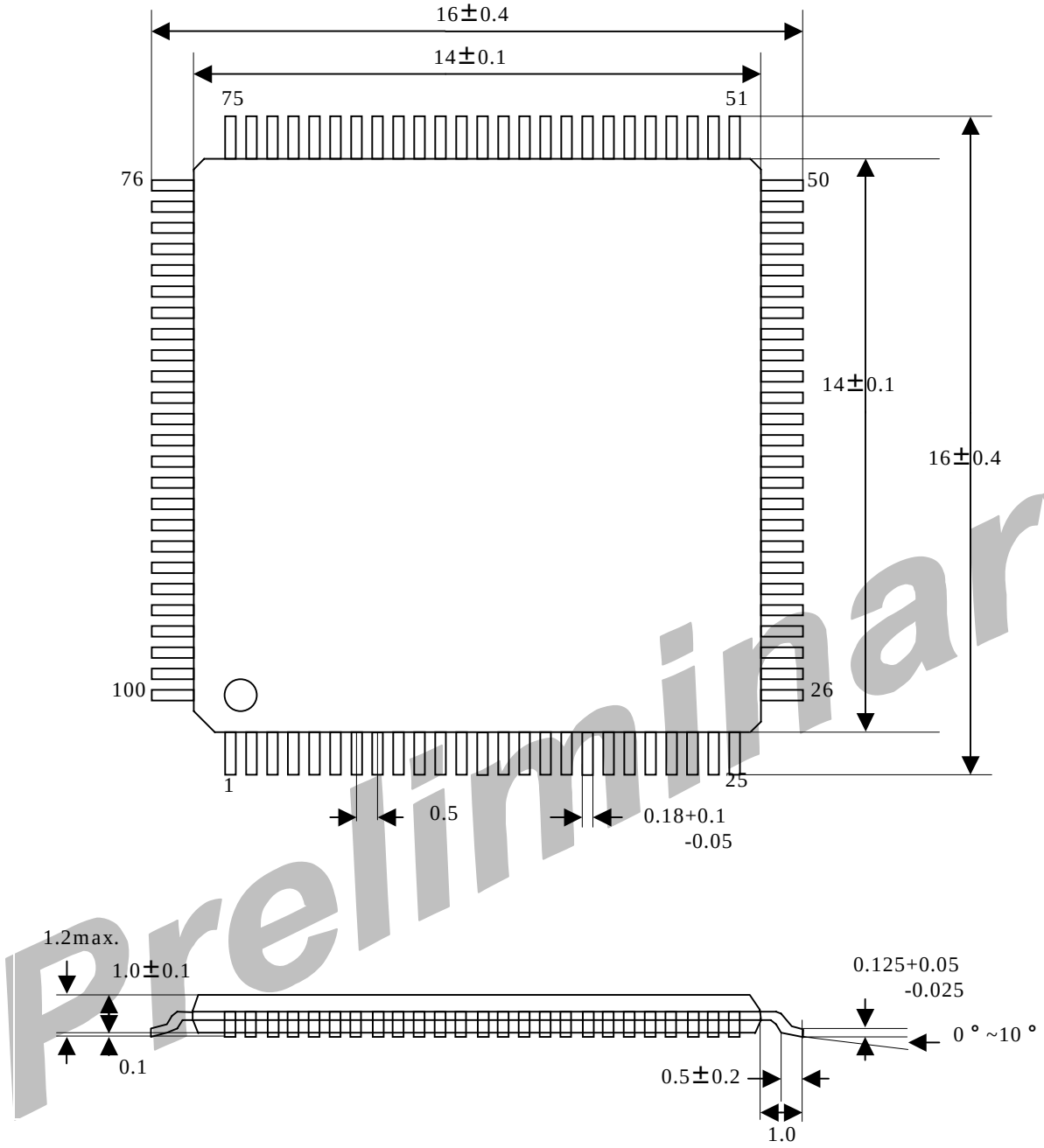


*Slave address=10000,CA1,CA0 (CA1,CA0 **are input terminals setting**)
*You should set register address with 8bit format.
*Data read is performed incremental based from set register address.

■ Example of peripheral circuit connection



■ Package



1. This data sheet may be changed without any notification for improvement.
2. We have no responsibility that this product may infringe any right.
3. No part of this document may be reproduced in any form without the prior written consent of us.