MS59402

CMOS Priority Interrupt Controller

■ Outline

- MS59402 is Interrupt Control LSI for MC68000CPU
- It is pin and function compatible to MC68153

■ Feature

- VME bus I / F possible
- MC68000 I / F possible
- 8 Read / Write registers
- 4 Interrupt request signals
- Each Interrupt request signals can permit / Inhibit individually
- 7 levels are able to set for each Interrupt request
- Interrupt vector can be set
- Interrupt vector output device is selectable
- Interrupt acknowledge daisy chaining
- 5volt power supply
- 40PIN PLASTIC DIP

■ Electrical definition

● Absolute maximum rating （Vss=0V）

Parameter	Symbol	Rated value	Unit
Supply voltage	V_{DD}	- 0.3 ~ 7.0	V
Input voltage	V_I	- 0.33 ~ V_{DD} + 0.5	V
Output voltage	V_O	- 0.33 ~ V_{DD} + 0.5	V
Output current	I_{OUT}	± 24	mA
Maximum power	P_D	200	mW
Supply current	I_{DD} / I_{SS}	± 40	mA
Storage Temperature	T_{STG}	- 65 ~ 150	°C

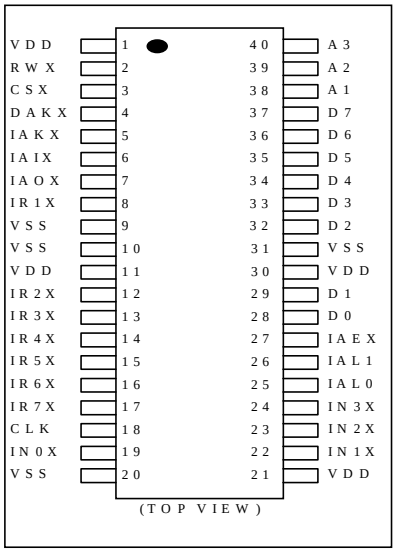
● Recommended operating condition （V_{SS}=0V）

Parameter	Symbol	Rated value			Unit
		MIN	TYP	MAX	
Operating voltage	V_{DD}	4.75	5.00	5.25	V
Input voltage	V_{IN}	V_{SS}	-	V_{DD}	V
Operating temperature	T_{OPr}	0	-	70	°C

● D.C. characteristics (Recommended operating condition)

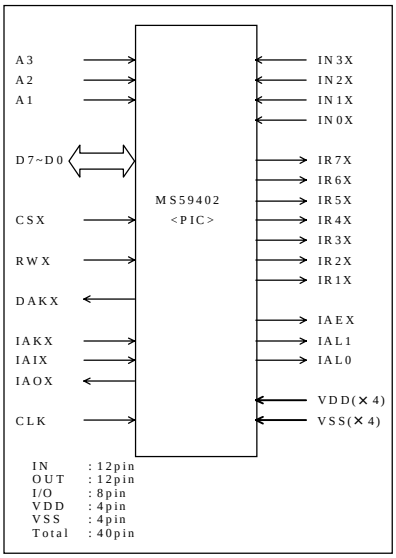
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Target PIN name
standby current	I_{DDS}	V_{IN} = V_{DD}orV_{SS} V_{DD} = MAX I_{OH} = I_{OL}=0	-	-	200	µA	
Input leakage current	I_L	V_{DD}=MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	- 1	-	1	µA	
tristate leakage current	I_{OZ}	V_{DD} = MAX V_{OH} = V_{DD} V_{OL} = V_{SS}	- 1	-	1	µA	D7, D6, D5, D4, D3, D2, D1, D0, DAKX, IR7X, IR6X, IR5X, IR4X, IR3X, IR2X, IR1X,
H level input voltage	V_{IH2}	TTL level V_{DD} = MAX	2.0	-	-	V	A3, A2, A1, D7, D6, D5, D4, D3, D2, D1, D0, CSX, RWX, IAKX, IAIX, IN3X, IN2X, IN1X, IN0X, CLK
L level input voltage	V_{IL2}	TTL level V_{DD} = MIN	-	-	0.8	V	
H level output voltage	V_{OH2}	V_{DD} = MIN I_{OH} = - 3mA	V_{DD} - 0.4	-	-	V	D7, D6, D5, D4, D3, D2, D1, D0, IA0X, IAEX, IAL1, IAL0
L level output voltage	V_{OL2}	V_{DD} = MIN I_{OL} = 6mA	-	-	V_{SS}+0.4	V	D7, D6, D5, D4, D3, D2, D1, D0, DAKX, IAOX, IR7X, IR6X, IR5X, IR4X, IR3X, IR2X, IR1X, IAEX, IAL1, IAL0
pull up resistor	R_{PU1}	V_{DD} = 5.0V	50	-	500	k Ω	A3, A2, A1, D7, D6, D5, D4, D3, D2, D1, D0, CSX, RWX, IAKX, IAIX, IN3X, IN2X, IN1X, IN0X

■ Terminal alignment



■ Terminal description

● Input output figure



■ Terminal function

PIN name	PIN No.	I/O	Polarity	Input level	Iol	Function
A3 A2 A1	40 39 38	I	True	TTL (with Pull_Up-R)		Address input Read/write cycle : Register address Interrupt acknowledge cycle : Interrupt level
D7~D0	37,36, 35,34, 33,32, 29,28	I/O	True	TTL (with Pull_Up-R)	6mA	Data bus Read / Write cycle : Register data Interrupt acknowledge cycle : Interrupt vector output
CSX	3	I	Low	TTL (with Pull_Up-R)		Chip select input
RWX	2	I		TTL (with Pull_Up-R)		read/write input 1：Read cycle 0：Write cycle
DAKX	4	O	Low		6mA	Data transfer acknowledge output (open drain) Read / Write cycle : Complete cycle Interrupt acknowledge cycle : Complete interrupt vector output
IAKX	5	I	Low	TTL (withPull_Up-R)		Interrupt acknowledge cycle
IAIX	6	I	Low	TTL (with Pull_Up-R)		Interrupt daisy chaining input 1：Exist higher priority interrupt 0：Nonexistent higher priority interrupt
IAOX	7	O	Low		6mA	Interrupt daisy chaining output 1：Not permit to lower priority device 0：Permit to lower priority device
IN3X IN2X IN1X IN0X	24 23 22 19	I	Low	TTL (with Pull_Up-R)		Interrupt request signal input
IR7X IR6X IR5X IR4X IR3X IR2X IR1X	17 16 15 14 13 12 8	O	Low		6mA	Interrupt request signals output (open drain) IR7X strong IR1X weak

PIN name	PIN No.	I/O	Polarity	Input level	Iol	Function
IAEX	27	O	Low		6mA	IAL output stable
IAL1 IAL0	26 25	O	True		6mA	Interrupt acknowledge number
CLK	18	I		TTL		Clock input（Max 25MHz）
VDD	1,11,21, 30					+ 5V power supply
VSS	9,10,20, 31					0V power supply

■ Register description

● Register map

Address	Register	Register bit								Initial	Function
A3 A2 A1	Name	7	6	5	4	3	2	1	0	value	
0 0 0	ICR0	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN0X control register
0 0 1	ICR1	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN1X control register
0 1 0	ICR2	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN2X control register
0 1 1	ICR3	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN3X control register
1 0 0	IVR0	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN0X vector register
1 0 1	IVR1	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN1X vector register
1 1 0	IVR2	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN2X vector register
1 1 1	IVR3	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN3X vector register

● Register bit function

Control register

FLG : Bit for TAS instruction of MC68000

FAC : Auto clear FLG bit

0 = No operation

1 = Auto reset FLG bit under interrupt acknowledge cycle

EIX : Select interrupt acknowledge response

0 = Internal response MS59402 will output interrupt vector and DAKX (data transfer acknowledge).

1 = External response MS59402 will not respond. External device which will output Interrupt request will output interrupt vector and DAKX.

IRE : permission of interrupt

0 = Inhibit

1 = Permit

IAC : Auto clear of TRE bit

0 = No operation

1 = Auto reset IRE bit under interrupt acknowledge cycle.

If you will permit interrupt request again, you will set IRE bit to “1” again.

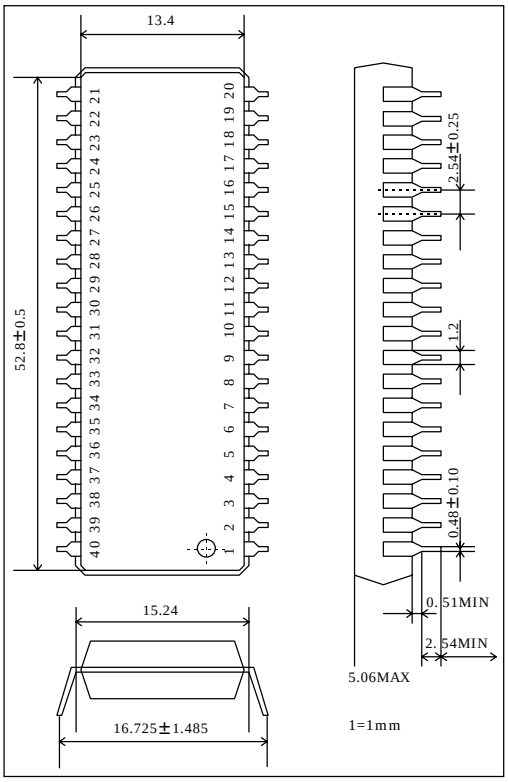
LV2 :
LV1 : } Interrupt request level
LV0 :

LV2	LV1	LV0	Correspond output
0	0	0	-
0	0	1	IR1X
0	1	0	IR2X
0	1	1	IR3X
1	0	0	IR4X
1	0	1	IR5X
1	1	0	IR6X
1	1	1	IR7X

Vector register

V7 ~ V0 : Interrupt vector
If ICR bit is “0”, these register value will appear to D7 to D0 PIN under interrupt acknowledge cycle.

- Package size



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