MS59402IP

Priority Interrupt Controller IP Module (Verilog-HDL)

■Outline

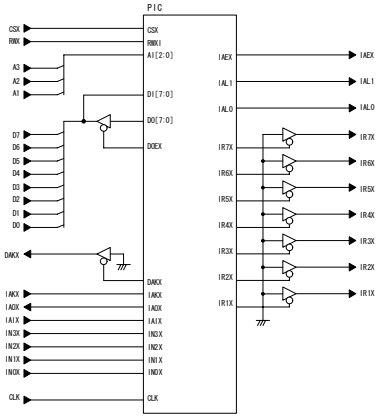
MS59402IP is Interrupt Control IP Module for MC68000CPU
Function compatible to MC68153

■Feature

- ●VME bus I／F possible
- ●MC68000 I／ F possible
- ●8read/write registers
- ●4 Interrupt request signals
- ●Each Interrupt request signals can permit/inhibit individually
- ●7 levels are able to set for each Interrupt request
- ●Interrupt vector can beset
- ●Interrupt vector output device is selectable
- ●Interrupt acknowledge daisy chaining

■Terminal description

●Input output figure

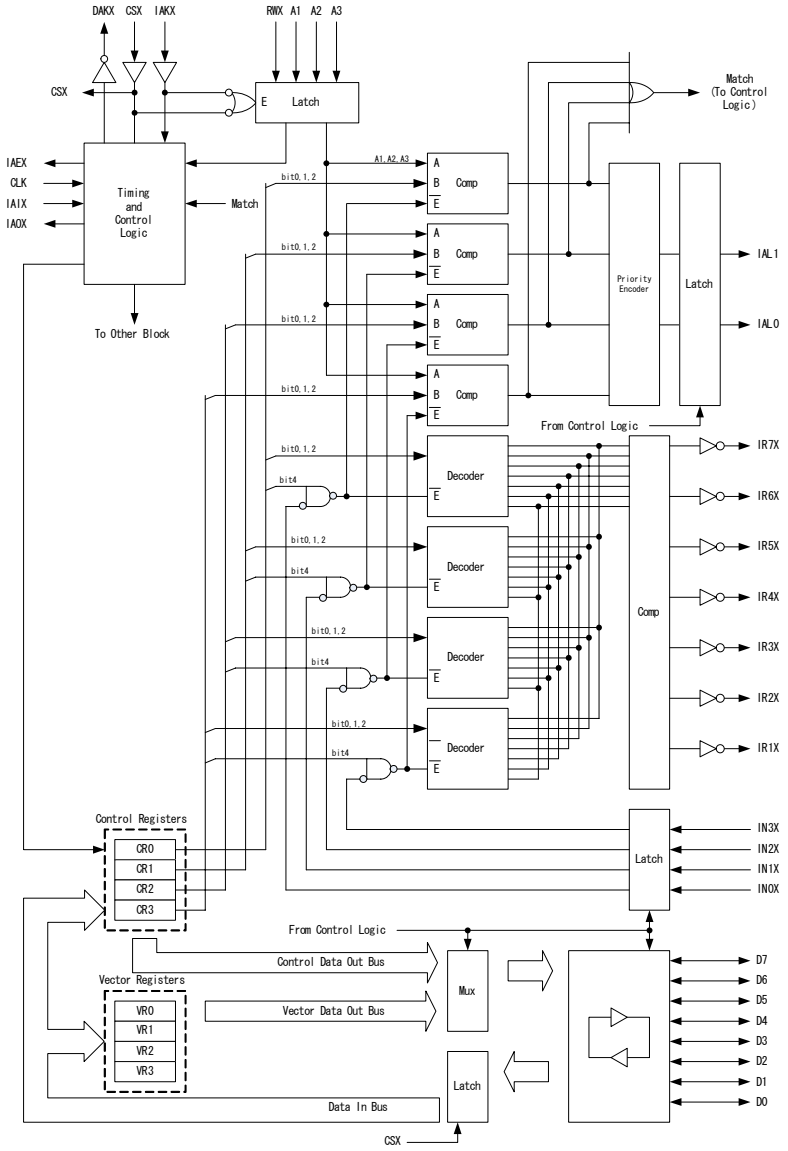


●Terminal function

PIN name	I/O	Polarity	Function
A3 A2 A1	I	True	Address input read/write cycle : register address interrupt acknowledge cycle : Interrupt level
D7~D0	I/O	True	Data bus read/write cycle : register data interrupt acknowledge cycle : interrupt vector output
CSX	I	Low	Chip select input
RWX	I		Read/Write input 1 : read cycle 0 : write cycle
DAKX	O	Low	Data transfer acknowledge output (open drain) read/write cycle : complete cycle interrupt acknowledge cycle : complete interrupt vector output
IAKX	I	Low	Interrupt acknowledge cycle
IAIX	I	Low	Interrupt daisy chaining input 1 : exist higher priority interrupt 0 : nonexistent higher priority interrupt
IAOX	O	Low	Interrupt daisy chaining output

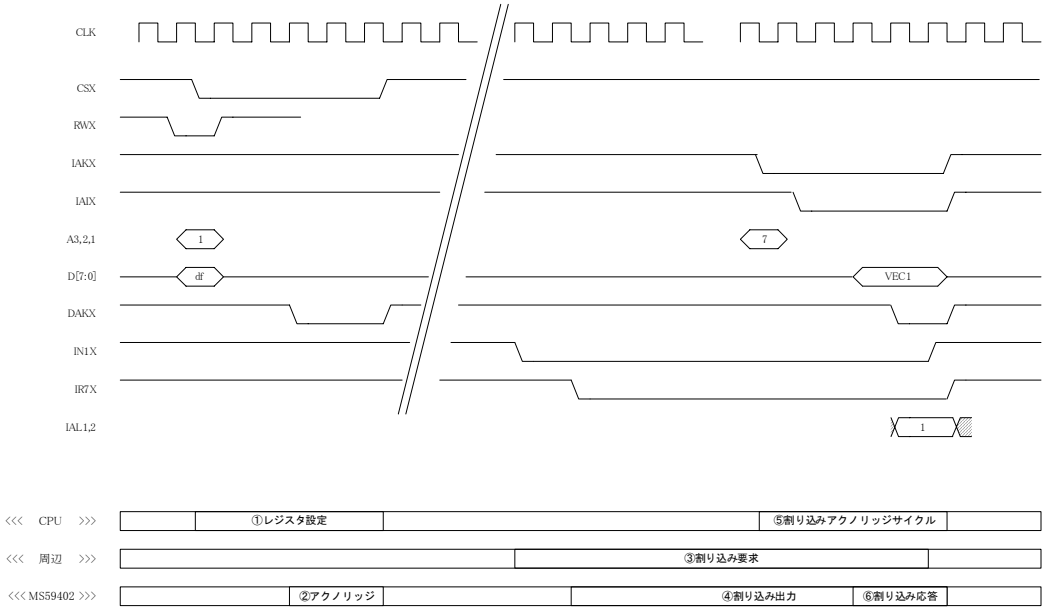
			1：not permit to lower priority device 0：permit to lower priority device
IN3X IN2X IN1X IN0X	I	Low	Interrupt request signal input
IR7X IR6X IR5X IR4X IR3X IR2X IR1X	O	Low	Interrupt request signals output (open drain) IR7X strong IR1X weak
IAEX	O	Low	IAL output stable
IAL1 IAL0	O	True	Interrupt acknowledge number
CLK	I		Clock input

■Block diagram



■Operating Description

Rough image Fig. corresponding to interrupt acknowledge operation



CLK～IAL1,2 are main input signals and <<< >>> show corresponding operation.

①CPU set interrupt level and vector output value on control register. In above figure IRC1 interrupt level is 7 which is corresponding to IN1X input.

②MS59402IP will output DAKX.

③When some device will output interrupt request, it is asserted IN1X Pin of MS59402IP in above Fig.

④Register setting data is equal to 7 corresponding to IN1X, so MS59402IP will output interrupt request output IR7X.

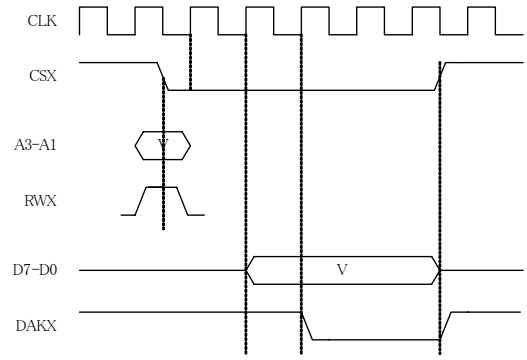
⑤CPU will be into acknowledge cycle when interrupt request signal from MS59402IP will be asserted.

⑥MS59402IP will respond to interrupt request, output VEC1 resister value, assert IAL1,2 to “01” corresponding to IN1X and assert DAKX.

■Timing chart

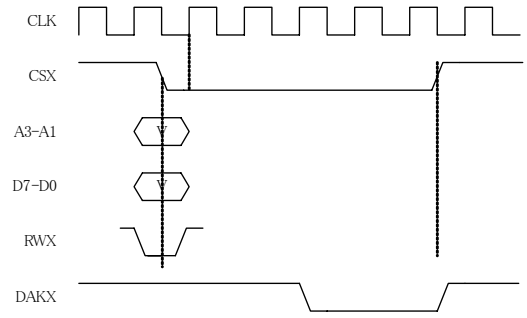
●I/O timing

●Read Cycle



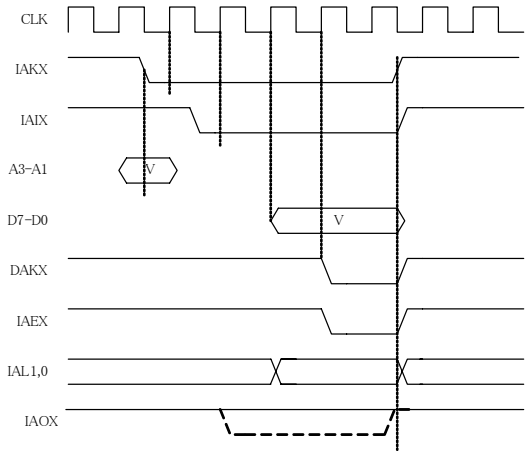
Address(A3-A1),Read/Write(RWX) will be latched at falling edge of CSX signal.

●Write Cycle



Address(A3-A1),data(D7-D0),Read/Write(RWX) will be latched at falling edge of CSX signal.

●Interrupt Acknowledge Cycle



Address(A3-A1) will be latched at falling edge of CSX signal.

■Register description

●Register map

Address	Register	Register bit								Initial	Function
A3 A2 A1	Name	7	6	5	4	3	2	1	0	value	
0 0 0	ICR0	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN0X control register
0 0 1	ICR1	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN1X control register
0 1 0	ICR2	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN2X control register
0 1 1	ICR3	FLG	FAC	EIX	IRE	IAC	LV2	LV1	LV0	00 Hex	IN3X control register
1 0 0	IVR0	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN0X vector register
1 0 1	IVR1	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN1X vector register
1 1 0	IVR2	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN2X vector register
1 1 1	IVR3	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	0F Hex	IN3X vector register

●Register bit function

・Control register

FLG : bit for TAS instruction of MC68000

FAC : Auto clear FLG bit

0= no operation

1= Auto reset FLG bit under interrupt acknowledge cycle

EIX : select interrupt acknowledge response

0= internal response MS59402 will output interrupt vector and DAKX (data transfer acknowledge).

1= external response MS59402 will not respond. External device which will output interrupt request will output interrupt vector and DAKX.

IRE : permission of interrupt

0= inhibit

1= permit

IAC : Auto clear of TRE bit

0= no operation

1= Auto reset IRE bit under interrupt acknowledge cycle.

If you will permit interrupt request again, you will set IRE bit to “1” again.

LV2 :
LV1 : } interrupt request level
LV0 :

LV2	LV1	LV0	correspond output
0	0	0	—
0	0	1	IR1X
0	1	0	IR2X
0	1	1	IR3X
1	0	0	IR4X
1	0	1	IR5X
1	1	0	IR6X
1	1	1	IR7X

・Vector register

V7～V0 : interrupt vector

If ICR bit is “0”, these register value will appear to D7 to D0 PIN under interrupt acknowledge cycle.

1.This datasheet may be changed without any notification for improvements.

2.Mega-sys Co., Ltd. have no responsibility that this product may infringe any right.

3.No part of this document may be reproduced in any form without the prior written consent of Mega-sys.Co.Ltd.