MS60201IP

HDLC Serial Commucatien Interface IP Module (verilog HDL)

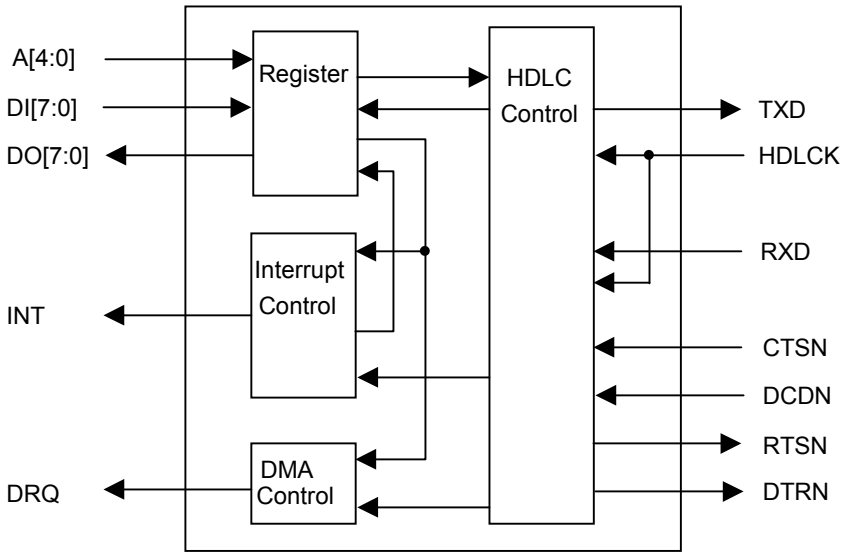
■ Outline

MS60201IP is IP module for HDLC (High level Data Link Control) communication interfaces.

■ Feature

- TX/RX FIFO.
- DMA controller.
- CRC-CCITT and CRC-16, two kinds of FCS is supported.
- Various interrupt request outputs.
- Loop back is possible.
- TX and RX common clock.

■ Block diagram



■ Input-and-output signal

Signal name	I/O	Polarity	Description
TXD	Output	-	TX data output
RXD	Input	-	RX data output
CTSN	Input	Low	CTS input
DCDN	Input	Low	DCD input
RTSN	Output	Low	RTS output
DTRN	Output	Low	DTR output
HDLCK	Input	-	Data transmission clock
RXINT	Output	HIgh	RX interrupt request
TXINT	Output	High	TX interrupt request
SPINT	Output	High	SP interrupt request
ESINT	Output	High	ES interrupt request
DRQT	Output	High	TX data DMA transfer request
DRQR	Output	High	RX data DMA transfer request
CK	Input	-	System clock input
RN	Input	Low	System reset input
DI[7:0]	Input	-	Write data input
DO[7:0]	Output	-	Read data output
AI[4:0]	Input	-	Address input
WR	Input	High	Data write strobe
RD	Input	High	Data read strobe

■ Register list

Address	R/W	Register name	Description
00	-	-	-
01	W	INTSTCL	interrupt request factor status clear
02	R/W	INTEN	interrupt request enable set
03	R/W	INTENCL	interrupt request enable clear
04	R/W	TRXINTEN	TX/RX interrupt request enable set
05	R/W	TRXINTENCL	TX/RX interrupt request enable clear
06	R/W	RXADDR	RX address set
07	R/W	RXCOND	RX operating condition set
08	R/W	RXTH	RX FIFO number (of row) when Interrupt request will be generated
09	R/W	RXINTS	RX interrupt request operation setup
0A	W	RXCTL	RX control register
0B	R	RXDATA	RX data register
0C	R/W	TXS	TX setting register
0D	R/W	TXTH	TX FIFO number (of row) when Interrupt request will be generated
0E	W	TXCTL	TX control register
0F	W	TXDATA	TX data register
10	R/W	MISC	Other setting register
11	R/W	DMAS	DMA setting register
12	R/W	PORTCTL	port output control register
13	-	-	-
14	-	-	-
15	-	-	-
16	R	ESINTST	ESINT factor status register
17	R	SPINTST	SPINT factor status register
18	R	NOINTST	Status register which are not interrupt request factors
19	R	RESIDUE	Status register of a fraction bit pattern
1A	R	TXST	TX status
1B	R	MON	Monitor register of interrupt request ports
1C	-	-	-
1D	-	-	-
1E	-	-	-
1F	W	SRST	Soft reset