MS60305

CMOS PIAFS INTERFACE LSI

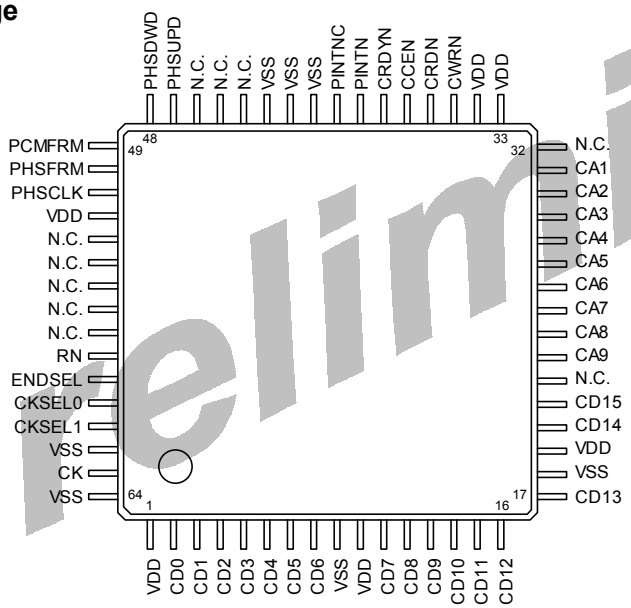
■ Outline

MS60305 is the 64kbps PIAFS communication control LSI.
This IC makes communication with PHS by 32Kbps or 64Kbps bearer data transfer.

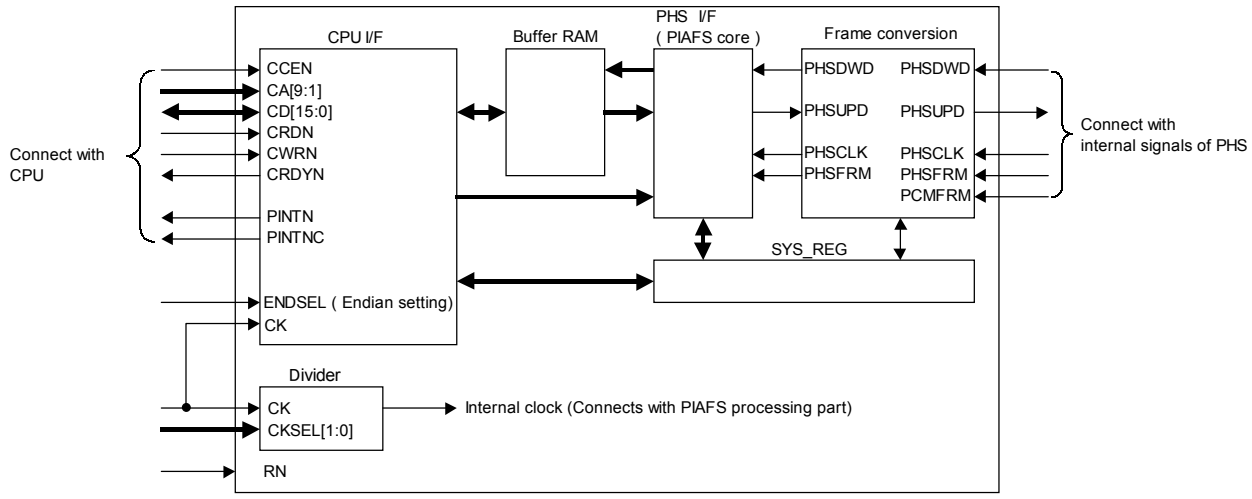
■ Feature

- PHS communication mode / PCM communication mode is selectable.
- Low power consumption by the clock divider circuit.
- Endian is selectable.
- Data conversion, transmission, and synchronous detection between CPU-PHS are performed.
- Data buffer is asynchronous 2port RAM (16bit*80 word).
- PHS TX and PHS RX interrupt request are provided.
- Power supply voltage is 3.0V or 3.3V Single power supply voltage.
- LQFP-64pin

■ Package



■ Block diagram



■ Input and output signal

Grouping	Signal name	I/O	Polarity	Description
CPU I/F	CCEN	I	"L" active	Connects with Chip select signal of CPU.
	CA[9:1]	I	-	Address input of CPU. (Only 16bit access, Operation of byte access is not guaranteed.)
	CRDN	I	"L" active	Connects with Read signal of CPU.
	CWRN	I	"L" active	Connects with Write signal of CPU.
	CD[15:0]	I/O		Data bus input and output of CPU.
	CRDYN	O	"L" active	Connects with Ready signal of CPU.
Interrupt	PINTN	O	"L" active , Open Drain	TX/RX interrupt request of PHS.
	PINTNC	O	"L"active , Complementary	TX/RX interrupt request of PHS.
PHS I/F	PHSCLK	I	Schmidt input	Bit clock input of PHS
	PHSFRM	I	Schmidt input	Frame input of PHS : 5ms cycle
	PCMFRM	I	Schmidt input	Frame input of PCM : 125µs cycle
	PHSDWD	I	-	RX data input
	PHSUPD	O	-	TX data output
Global	CK	I	Schmidt input	Clock of this LSI. Frequency range is 6MHz to 20MHz.
	RN	I	"L" active , Schmidt input	Asynchronous reset input.
ModeSet	CKSEL[1:0]	I	-	Setup of Internal clock divider ratio. CKSEL[1:0] = (H , H) : 1/1 (H , L) : 1/2 (L , H) : 1/3 (L , L) : 1/4
	ENDSEL	I	PullUp	Change of Endian of CPUI/F. H : Little Endian L : Big Endian

■ Electrical definition

● Absolute maximum rating (Vss=0V)

Parameter	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.3 ~ 4.0	V
Input voltage	V_{IN}	-0.3~ V_{DD} + 0.5	V
Output current	I_{OUT}	± 3.0	V
Storage Temperature	T_{STG}	- 55 ~ +125	° C

● Recommended operating condition（Vss=0V）

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0 2.7	3.3 3.0	3.6 3.3	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating Temperature	Topr	- 40	-	85	°C

● D.C. characteristics

TBD

■ Register / Memory map

- Address 0x000 ~ 0x0FFh is SYSREG.
- Address 0x100 ~ 0x1FFh is PHSREG.
- Address 0x200 ~ 0x3FFh is PHSBUF.

● SYSREG (System control register) field

Address	Register name								
0x000h	MODE	15	14	13	12	11	10	9	8
		-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-
		7	6	5	4	3	2	1	0
		PCMPHS	64K32K	-	-	-	PPOS2	PPOS1	PPOS0
		R/W(0)	R/W(0)	-	-	-	R/W(0)	R/W(0)	R/W(0)
0x004h	PHSDLY	15	14	13	12	11	10	9	8
		-	-	-	-	-	-	PHSDLY9	PHSDLY8
		-	-	-	-	-	-	R/W(0)	R/W(0)
		7	6	5	4	3	2	1	0
		PHSDLY7	PHSDLY6	PHSDLY5	PHSDLY4	PHSDLY3	PHSDLY2	PHSDLY1	PHSDLY0
		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

● PHSREG (PHS I/F control register) field

Address	Register name								
0x100h	TXCNT	15	14	13	12	11	10	9	8
		-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-
		7	6	5	4	3	2	1	0
		FINTE	RTMOD	-	-	-	-	TPC	TXE
		R/W(0)	R/W(0)	-	-	-	-	R/W(0)	R/W(0)
0x104h	RXCNT	15	14	13	12	11	10	9	8
		-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-
		7	6	5	4	3	2	1	0
		RINTE	-	-	-	-	-	-	RXE
		R/W(0)	-	-	-	-	-	-	R/W(0)
0x108h	STATUS	15	14	13	12	11	10	9	8
		7	6	5	4	3	2	1	0
		RINT	CRCER	RPE	RES	FINT	TXOUT	TPE	TES
		R/W(x)	R(x)	R(x)	R(x)	R/W(x)	R(x)	R(x)	R(x)
0x10Ch	TESTPF	15	14	13	12	11	10	9	8
		-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-
		7	6	5	4	3	2	1	0
		TESTPF	-	-	-	-	-	-	TEST1
		R/W(0)	-	-	-	-	-	-	R/W(0)

●PHSBUF field

Address	bit15 … … bit0
0x3FFh 0x3A0h	Not inplemented (96Byte)
0x39Fh 0x350h	RX buffer B (80Byte)
0x34Fh 0x300h	RX buffer A (80Byte)
0x200h 0x2A0h	Not inplemented (96Byte)
0x29Fh 0x250h	TX buffer B (80Byte)
0x24Fh 0x200h	TX buffer A (80Byte)

■ Register function

● SYSREG (System control register) field

MODE (0x000h)

PCMPHS	:	Communication interface mode setting
64K32K	:	PCM communication speed setting
PPOS[2:0]	:	PCM RX data arrangement setting

PHSDLY(0x004h)

PHSDLY[9:0]	:	PHS TX delay setting

● PHSREG (PHS I/F control register) field

TXCNT (0x100h)

FINTE	:	PHS interrupt enable
RTMOD	:	PHS real time transmission mode select
TPC	:	PHS TX buffer select
TXE	:	PHS TX enable

RXCNT (0x104h)

RINTE	:	PHS frame data RX completed interrupt enable
RXE	:	PHS frame data RX enable

STATUS (0x108h)

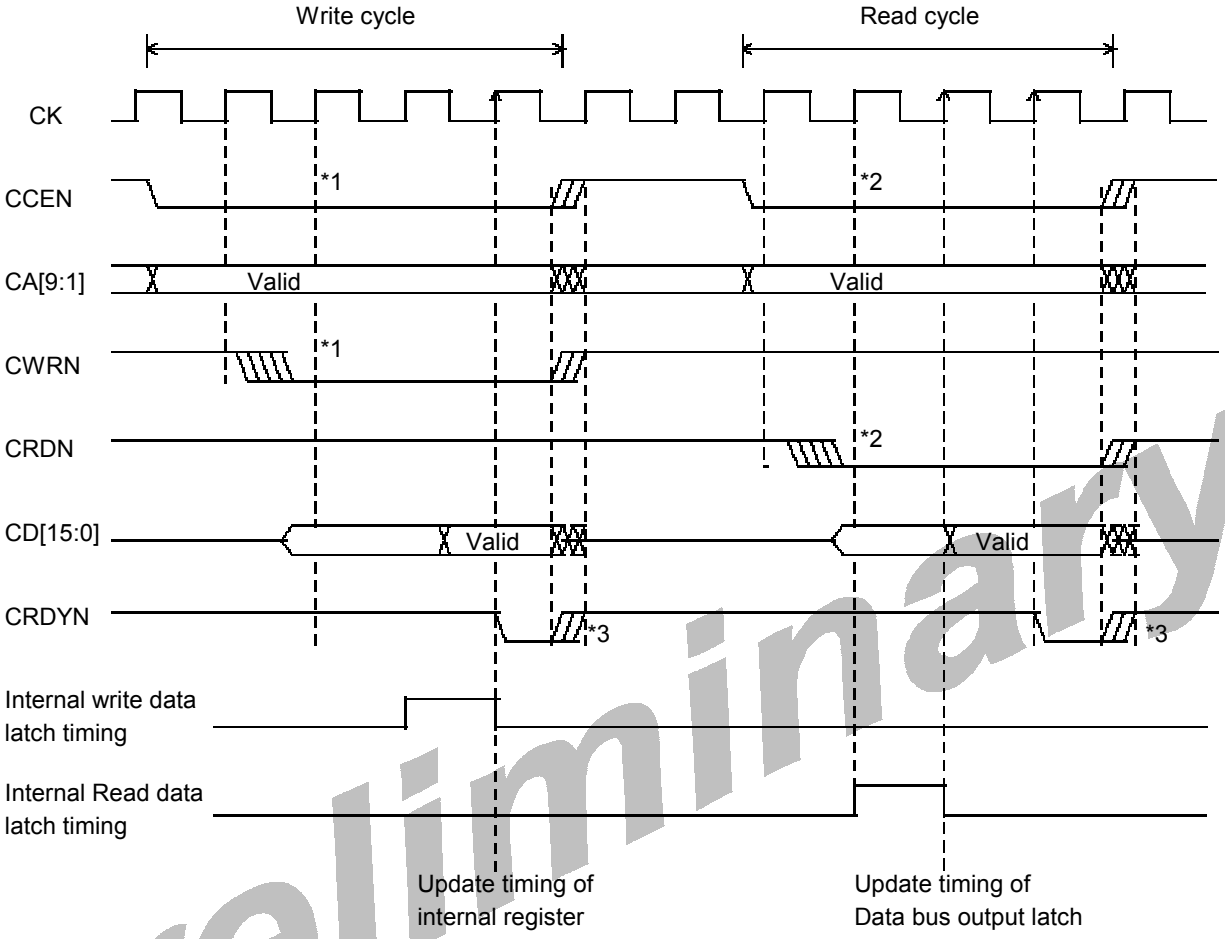
RINT	:	RX completed interrupt status of "Frame data for PHS RX"
CRCER	:	PHS RX data frame CRC check result
RPE	:	PHS RX data storing buffer
RES	:	PHS RX display
FINT	:	Interrupt status in every 640 bits for PHS TX
TXOUT	:	Status during PHS TX.
TPE	:	PHS write enable TX buffer.
TES	:	PHS TX display

TESTPF (0x10Ch)

TESTPF	:	PHS test setting
TES1	:	PHS test setting

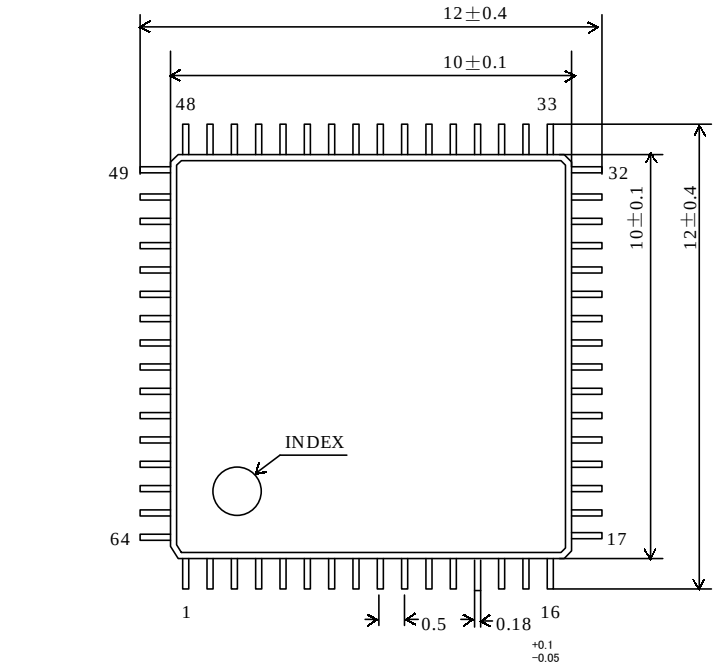
■ CPU bus interface

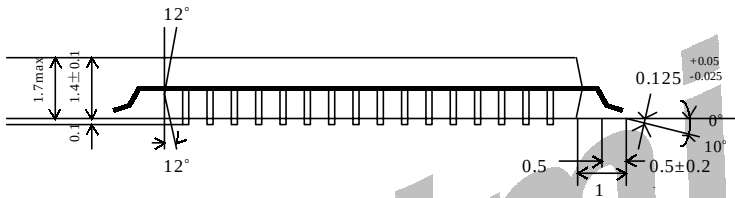
Timing of CPU bus interface is shown.
"Write operation" and "Read operation" are performed by synchronizing with system clock (CK) inside LSI.
Therefore,Wait cycle occurs at every R/W of all registers and RAM.



***1 :** At the time of rising edge CK, when condition CCEN="L" & CWRN="L" is detected, "Write access" is started.
***2 :** At the time of rising edge CK, when condition CCEN="L" & CRDN="L" is detected, "Read access" is started.
***3 :** CRDYN assertion is performed on rising edge of CK by the internal sequence. When the conditions of *1 or *2 is not approved, CRDN negates asynchronously to CK.

■ Package size





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