MS69701

CMOS PIAFS INTER FACE LSI

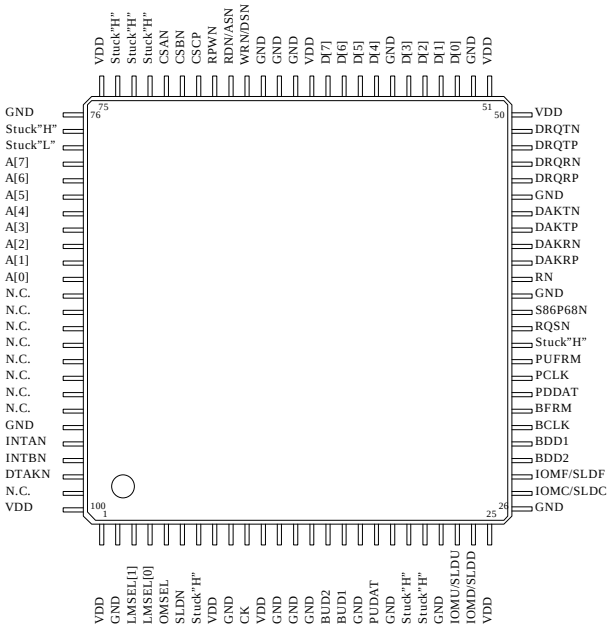
■ Outline

- MS69701 is Communication control LSI for PIAFS.
- Tx-Rx frame buffer, Automatic generating / checking circuit of CRC is implemented.
- PIAFS, 32Kbps bearer transmission, and connection with an ISDN network are possible.

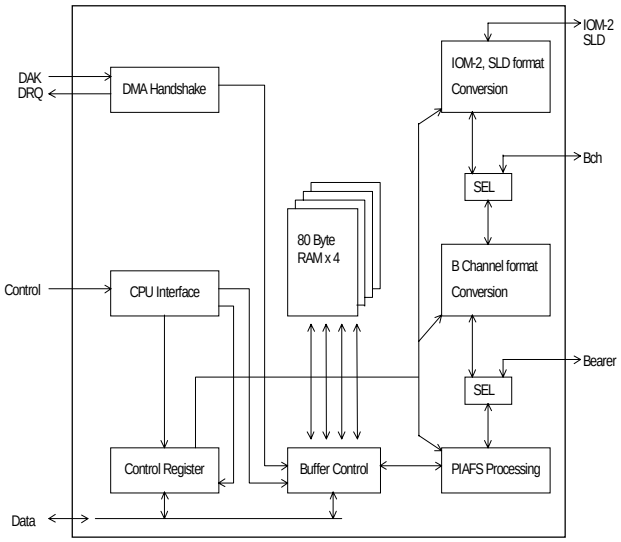
■ Feature

- Frame buffer is implemented.
- Automatic generating / checking CRC.
- It supports 8 bits data bus
- Both CPU interface are possible for 86 system and 68 system.
- Two interrupt request outputs of Tx-Rx are provided.
- Power supply voltage : 5.0V single or 3.3V single or 3.0V single.
- CMOS process.
- Sleep mode function.
- 100PIN's plastic QFP package.

■ Package



■ Block diagram



■ Input and output signal

Signal name	I/O	Polarity	Description
CSAN	I	Low	Chip select A
CSBN	I	Low	Chip select B "AND" of A, B and C are Internal domain Chip select
CSCP	I	High	Chip select C
A[7:0]	I	-	Internal register select address
RWN	I	-	Read/Write status signal input for 68 system CPU (Fixes to "High" at the time of 86 system mode.)
RDN	I	Low	Read strobe (Case of 68 system mode, Address strobe input)
WRN	I	Low	Write strobe (Case of 68 system mode, Data strobe input)
D[7:0]	I/O	-	Data input and output Bus
DTAKN	O	Low	Data Acknowledge
INTAN	O	Low	TX interrupt output (Open drain)
INTBN	O	Low	RX interrupt output (Open drain)
DRQTN	O	Low	TX data transmission request (polarity Low)
DRQTP	O	High	TX data transmission request (polarity High)
DAKTN	I	Low	TX data transmission Acknowledge (polarity Low) *If not use, fixes to "HIGH"
DAKTP	I	High	TX data transmission Acknowledge (polarity High) *If not use, fixes to "Low"
DRQRN	O	Low	RX data transmission request (polarity Low)
DRQRP	O	High	RX data transmission request (polarity High)
DAKRN	I	Low	RX data transmission Acknowledge (polarity Low) * If not use, fixes to "HIGH"
DAKRP	I	High	RX data transmission Acknowledge (polarity High) * If not use, fixes to "Low"
PUFRM	I	High	Up frame (PHS) * If not use, fixes to "Low"
PCLK	I	-	Bit clock (PHS) * If not use, fixes to "Low"
PDDAT	I	High	Down data (PHS) * If not use, fixes to "Low"
PUDAT	O	High	Up data (PHS)
BFRM	I	High	8Khz (B ch) * If not use, fixes to "Low"
BCLK	I	-	64Khz (B ch) * If not use, fixes to "Low"
BDD1	I	High	Down-1 (B ch) * If not use, fixes to "Low"
BUD1	O	High	Up-1 (B ch)
BDD2	I	High	Down-2 (B ch) * If not use, fixes to "Low"
BUD2	O	High	Up-2 (B ch)
IOMF/SLDF	I	High	8Khz frame (IOM-2) / 8Khz frame (SLD)
IOML/SLDL	I	-	Double speed clock (IOM-2) / 512K bit clock (SLD)
IOMD/SLDD	I	High	Down data (IOM-2) / Line out (SLD)
IOMO/SLDU	O	High	Up data (IOM-2) / Line in (SLD)
S86P68N	I	-	86 system CPU interface / 68 system CPU interface select
LMSEL[1:0]	I	-	Operation Mode set (PHS / B channel / IOM-2 or SLD)
OMSEL	I	-	Output function select open drain / three state
SLDN	I	Low	Select IOM-2 or SLD (SLD is LOW)
RQSN	I	-	DMA, DRQ style select Level or Edge (Level is High)
CK	I	-	System clock (max : 16Mhz / recommended : 10Mhz)
RN	I	Low	System reset

■ Electrical definition

● Absolute maximum rating (Vss=0V)

Parameter	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.3 ~ 6.0	V
Input voltage	V_{IN}	-0.3 ~ V_{DD} + 0.5	V
Output current	I_{OUT}	± 25	mA
Storage Temperature	T_{STG}	- 65 ~ 150	° C

● Recommended operating condition（Vss=0V）

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.5 3.0 2.7	5.0 3.3 3.0	5.5 3.6 3.3	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating Temperature	Topr	- 40	-	85	°C

● D.C. characteristics

5V ± 0.5V, VSS = 0V, Ta = - 40 ~ 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{STP}	Standby state			400	μA
Input leakage Current	I_L	-	-1		1	μA
Tristate leakage Current	I_{OZ}	-	-1		1	μA
Output voltage	V_{OH} V_{OL}	I = standard current value I = standard current value	V_{DD} - 0.4 -	- -	- 0.4	V V
Input voltage (Except Schmidt)	V_{IH} V_{IL}	V_{DD} = 5.5V V_{DD} = 4.5V	3.5 -	- -	- 1.0	V V
Input voltage (Schmidt terminal)	V_{TH} V_{TL}	V_{DD} = 5V V_{DD} = 5V	4.0 -	- -	- 0.8	V V
Pull up resistor	R_{PU}	V_I = 0V	50	100	200	K Ω
Pull down resistor	R_{PD}	V_I = V_{DD}	50	100	200	K Ω
Terminal capacitance	C_{IO}	f = 1Mhz	-	-	12	PF

3.3V ± 0.3V, VSS = 0V, Ta = - 40 ~ 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{STP}	Standby state	-	-	300	μA
Input leakage Current	I_L	-	-1	-	1	μA
Tristate leakage Current	I_{OZ}	-	-1	-	1	μA
Output voltage	V_{OH} V_{OL}	I = standard current value I = standard current value	V_{DD} - 0.3 -	- -	- 0.3	V V
Input voltage (Except Schmidt)	V_{IH} V_{IL}	V_{DD} = 3.6V V_{DD} = 3.0V	2.2 -	- -	- 0.8	V V
Input voltage (Schmidt terminal)	V_{TH} V_{TL}	V_{DD} = 3.3V V_{DD} = 3.3V	2.4 -	- -	- 0.6	V V
Pull up resistor	R_{PU}	V_I = 0V	90	180	360	K Ω
Pull down resistor	R_{PD}	V_I = VDD	90	180	360	K Ω
Terminal capacitance	C_{IO}	f = 1Mhz	-	-	12	PF

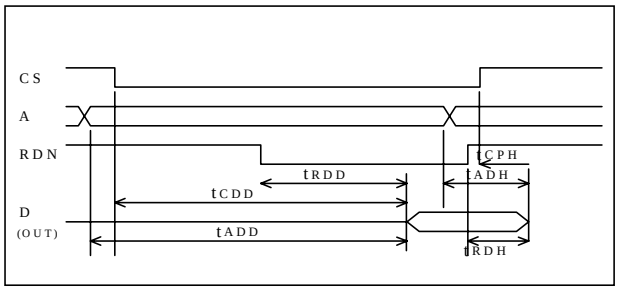
3V ± 0.3V, VSS = 0V, Ta = - 40 ~ 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{STP}	Standby state	-	-	260	μA
Input leakage Current	I_L	-	-1	-	1	μA
Tristate leakage Current	I_{OZ}	-	-1	-	1	μA
Output voltage	V_{OH} V_{OL}	I = standard current value I = standard current value	V_{DD} - 0.3 -	- -	- 0.3	V V
Input voltage (Except Schmidt)	V_{IH} V_{IL}	V_{DD} = 3.6V V_{DD} = 3.0V	2.0 -	- -	- 0.8	V V
Input voltage (Schmidt terminal)	V_{TH} V_{TL}	V_{DD} = 3.3V V_{DD} = 3.3V	2.3 -	- -	- 0.5	V V
Pull up resistor	R_{PU}	V_I = 0V	100	200	400	K Ω
Pull down resistor	R_{PD}	V_I = VDD	100	200	400	K Ω
Terminal capacitance	C_{IO}	f = 1Mhz	-	-	12	PF

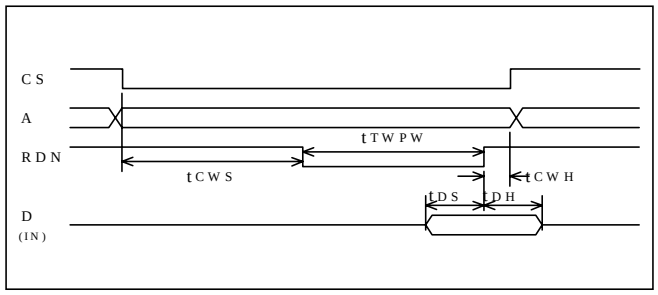
● A.C. characteristics

 # 86 MODE

• Read cycle

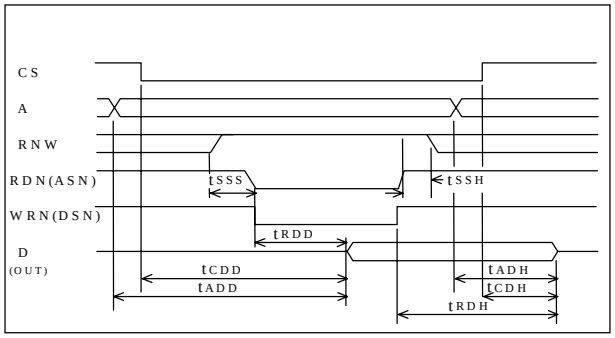


• Write cycle

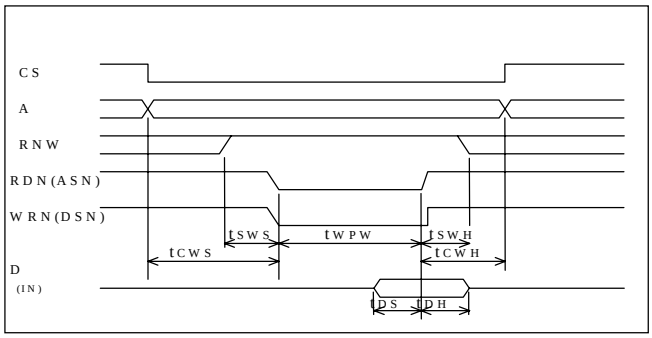


 # 68 MODE

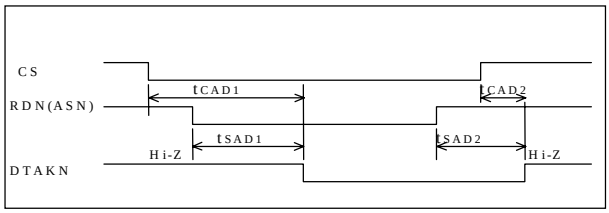
• Read cycle



• Write cycle



• Data Acknowledge Timing



• Read cycle

Symbol	Content	Min	Typ	Max	Unit
tCDD	Chip select - Data delay	-	-	80	nsec
tADD	Address - Data delay	-	-	80	nsec
tRDD	Read strobe - Data delay	-	-	40	nsec
tCDH	Chip select - Data hold	-	-	30	nsec
tADH	Address - Data hold	-	-	30	nsec
tRDH	Read strobe - Data hold	-	-	30	nsec
tSSS	RWN - Strobe set up time	10	-	-	nsec
tSSH	RWN - Strobe hold time	10	-	-	nsec

• Write cycle

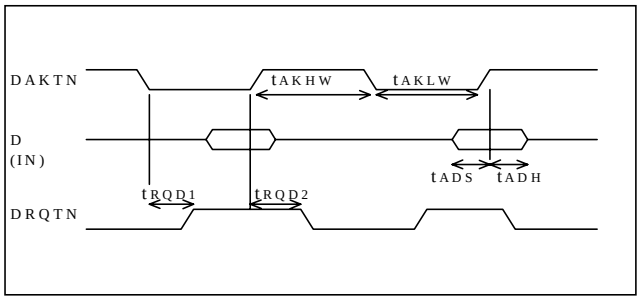
Symbol	Content	Min	Typ	Max	Unit
tCWS	Chip select (Address) - Write strobe set up time	30	-	-	nsec
tWPW	Write strobe pulse width	30	-	-	nsec
tCWH	Chip select (Address) - Write strobe hold time	0	-	-	nsec
tDS	Write data set up time	20	-	-	nsec
tDH	Write data hold time	0	-	-	nsec
tSWS	RWN - Strobe set up time	5	-	-	nsec
tSWH	RWN - Strobe hold time	5	-	-	nsec

• Data Acknowledge

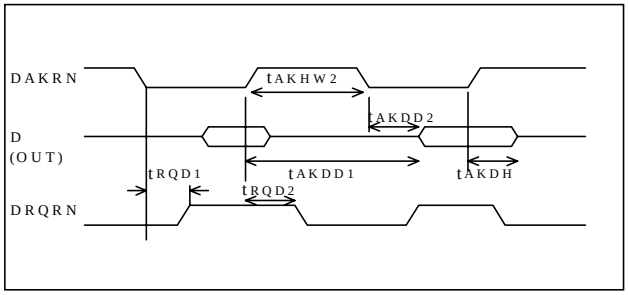
Symbol	Content	Min	Typ	Max	Unit
tCAD1	Chip select - Acknowledge delay 1	-	-	30	nsec
tSAD1	Strobe - Acknowledge delay 1	-	-	30	nsec
tCAD2	Chip select - Acknowledge delay 2	-	-	30	nsec
tSAD2	Strobe - Acknowledge delay 2	-	-	30	nsec

● DMA cycle

• Write cycle (TX)



• Read cycle (RX)



• Write cycle

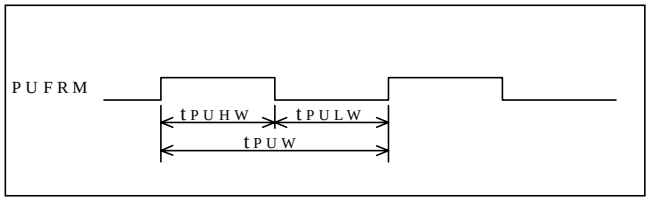
Symbol	Content	Min	Typ	Max	Unit
tRQP1	Acknowledge - Request delay 1	-	-	30	nsec
tRQD2	Acknowledge - Request delay 2	-	-	30	nsec
tAKHW	Acknowledge non active width	40	-	-	nsec
tAKLW	Acknowledge active width	40	-	-	nsec
tADS	Acknowledge - Data set up time	20	-	-	nsec
tADH	Acknowledge - Data hold time	0	-	-	nsec

• Read cycle

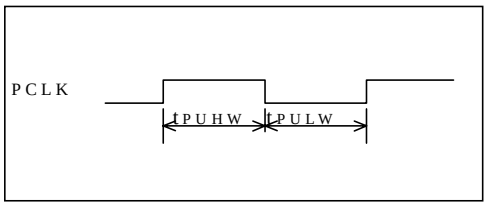
Symbol	Content	Min	Typ	Max	Unit
tRQD1	Acknowledge - Request delay 1	-	-	30	nsec
tRQD2	Acknowledge - Request delay 2	-	-	30	nsec
tAKHW2	TX Acknowledge non active width	30	-	-	nsec
tAKDD1	TX Acknowledge - Request delay 1	-	-	80	nsec
tAKDD2	TX Acknowledge - Request delay 2	-	-	40	nsec
tAKDH	Acknowledge - Output data hold time	-	-	30	nsec

● PHS Interface

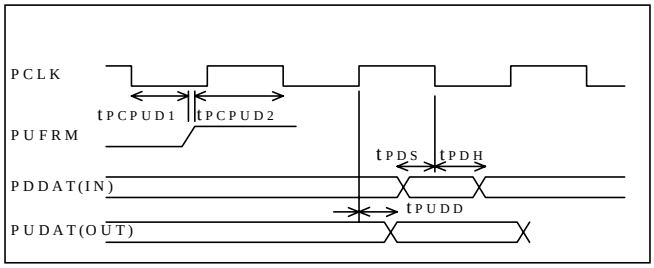
• Frame signal



• Bit Clock

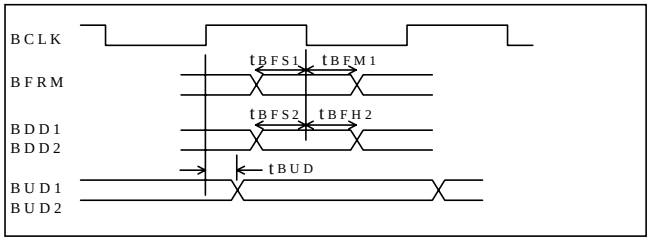


• Data input and output



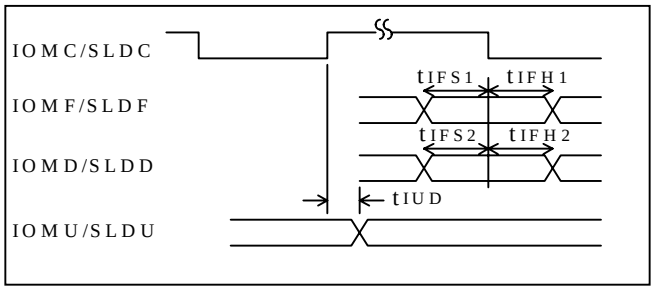
Symbol	Content	Min	Typ	Max	Unit
tPUW	PHS frame cycle	-	160	-	PCLK
tPUHW	PHS frame "High" period	12	-	-	CK
tPULW	PHS frame "Low" period	12	-	-	CK
tPCKHW	PHS Bit clock "High" period	12	-	-	CK
tPCKLW	PHS Bit clock "Low" period	12	-	-	CK
tPCPUD1	PHS Bit clock - Frame delay 1	12	-	-	CK
tPCPUD2	PHS Bit clock - Frame delay 2	12	-	-	CK
tPDS	PHS Down data set up time	12	-	-	CK
tPDH	PHS Down data hold time	12	-	-	CK
tPUDD	PHS Up data output delay	-	-	10	CK

● B ch Interface



Symbol	Content	Min	Typ	Max	Unit
t_{BFS1}	B ch Frame set up time	20	-	-	nsec
t_{BFH1}	B ch Frame hold time	20	-	-	nsec
t_{BFS2}	B ch Down data set up time	20	-	-	nsec
t_{BFH2}	B ch Down data hold time	20	-	-	nsec
t_{BUD}	B ch Up data output delay	-	-	40	nsec

● IOM-2, SLD Interface



Symbol	Content	Min	Typ	Max	Unit
t_{IFS1}	IOM Frame set up time	20	-	-	nsec
t_{IFH1}	IOM Frame hold time	20	-	-	nsec
t_{IFS2}	IOM Down data set up time	20	-	-	nsec
t_{IFH2}	IOM Down data hold time	20	-	-	nsec
t_{IUD}	IOM Up data output delay	-	-	40	nsec

■ Register

- Address 00 ~ 4BH is TX Data buffer.
- Address 80 ~ CFH is RX Data buffer.
- Address E0 ~ EEH is control register (Refer to following tables).

Address	Register name	b7	b6	b5	b4	b3	b2	b1	b0
E0H	TX Control	TSCLR WR	TFCLR WR	TECLR WR	-	-	-	TFENA R/W	TEC R/W
E1	TX Status	TSTS RD	TFLG RD	-	-	-	-	TUR RD	TES RD
E2	RX Control	RSCLR WR	RFCLR WR	-	-	-	-	RFENA R/W	REC R/W
E3	RX Status	RSTS RD	RFLG RD	RCERR RD	-	-	-	RUR RD	RES RD
E4	Interrupt-request Control	-	TCIE R/W	TDIE R/W	TSIE R/W	-	-	RDIE R/W	RSIE R/W
E5	Interrupt-request Status	-	TCIF RD	TDIF RD	TSIF RD	-	-	RDIF RD	RSIF RD
E6	DMA Control	TADE R/W	TDMAC WR	TDMAB WR	TDCLR WR	RADE R/W	RDMAC WR	RDMAB WR	RDCLR WR
E7	DMA Status	-	-	TDMAS RD	-	-	-	RDMAS RD	-
E8	Layer1 Control	-	-	-	-	-	BBSEL R/W	B1E R/W	B2E R/W
E9	Blank	-	-	-	-	-	-	-	-
EA	IOM Control	CHC2 R/W	CHC1 R/W	CHC0 R/W	-	CHN2 R/W	CHN1 R/W	CHN0 R/W	-
EB	IOM Status	-	-	-	-	-	-	-	SLD RD
EC	Mode Select	-	-	-	-	-	-	LMSR1 R/W	LMSR0 R/W
ED	Mode Status	-	-	-	-	-	-	LMSP1 RD	LMSP0 RD
EE	LSI Control	-	-	-	-	-	LOOP R/W	SLEEP R/W	RESET R/W

E0H

TSCLR : TSTS clear
TFCLR : TFLG clear
TECLR : TX End interrupt request clear
TFENA : TFLG Set enable
TEC : TX Enable

E1H

TSTS : TX Buffer status
TFLG : TX Flag
TUR : TX Under run
TES : Carrying on transmission Status

E2H

RSCLR : RSTS clear
RFCLR : RFLG clear
RFENA : RFLG Set enable
REC : RX Enable

E3H

RSTS : RX Buffer transmission status
RFLG : RX Flag
RCERR : RX CRC Error
RUR : RX Under run
RES : Carrying on Receving Status

E4H

TCIE : TX End interrupt request enable
TDIC : TX DMA End interrupt request enable
TSIE : TX Forwarding interrupt request enable
RDIE : RX DMA End interrupt request enable
RSIE : RX Transmission interrupt request enable

E5H

TCIF	: TX End interrupt request Flag	RDIF	: RX DMA End interrupt request Flag
TDIF	: TX DMA End interrupt request Flag	RSIF	: RX Transmission interrupt request Flag
TSIF	: TX Forwarding interrupt request Flag		

E6H

TADE	: TX DMA Automatic start enable	RADE	: RX DMA Automatic start enable
TDMAC	: TX DMA Start	RDMAC	: RX DMA Start
TDMAB	: TX DMA Stop	RDMAB	: RX DMA Stop
TDCLR	: TX DMA End interrupt request clear	RDCLR	: RX DMA End interrupt request clear

E7H

TDMAS	: TX DMA status	RDMAS	: RX DMA status

E8H

BBSEL	: PHS - Bch Data position set
B1E	: B1 Channel connection permission
B2E	: B2 Channel connection permission

EAH

CHC (2:0): Number of IOM-2 multi frames setting
CHN (2:0): Frame number setting for IOM-2

EBH

SLD	: IOM-2 / SLD Mode status

ECH

LMSR (1:0)	: Layer1 Mode set

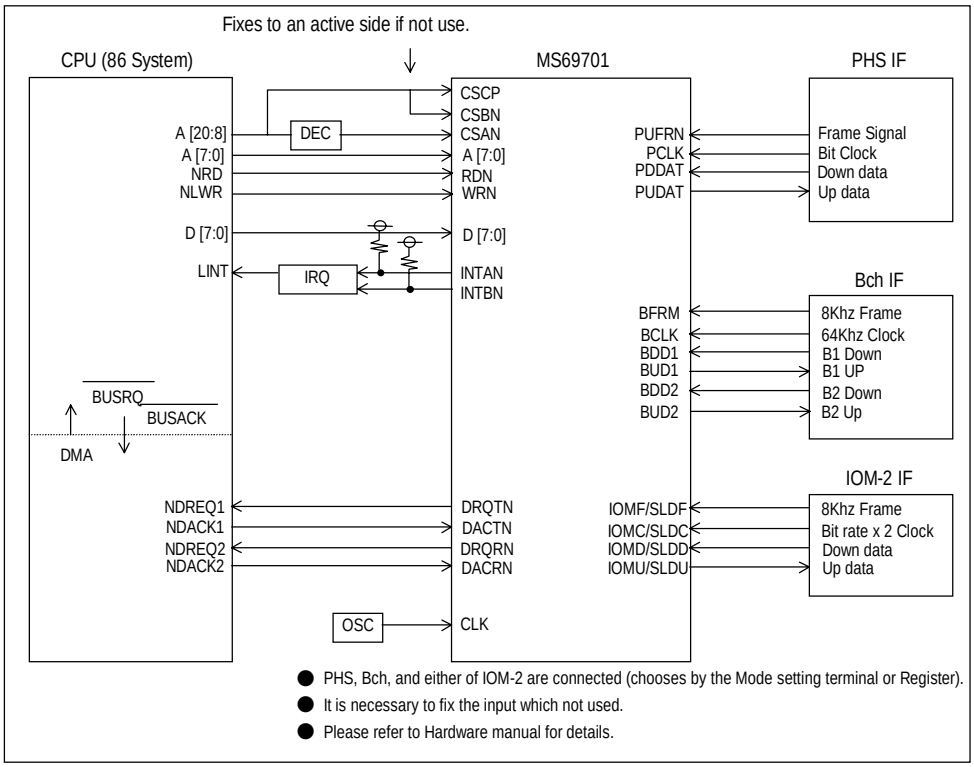
EDH

LMSP (1:0)	: Layer1 Mode set status

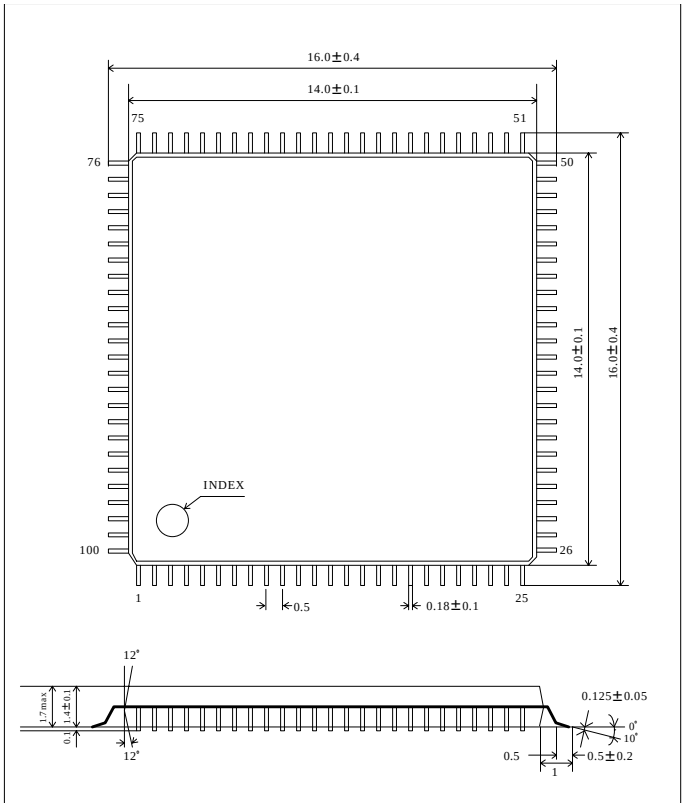
EEH

LOOP	: Loop back set
SLEEP	: Sleep mode set
RESET	: Soft reset

■ Example of peripheral circuit connection



■ Package size



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