MS70201IP

YUV to RGB Conversion IP module (Verilog HDL)

■ Outline

MS70201IP is IP module which changes YUV image data signal to RGB image data signal.

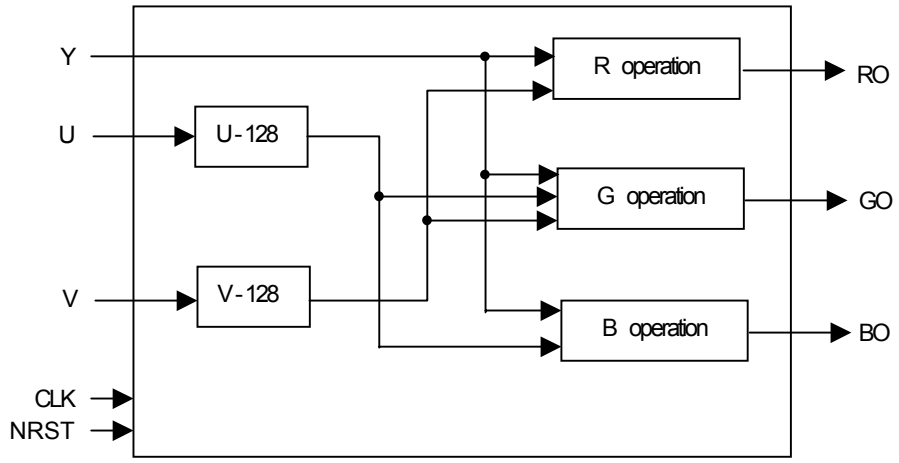
■ Feature

- Input and output data width 8 bits.
- High speed pipeline operation processing.
- Compatible with Conversion operation ITU-RBT-601.

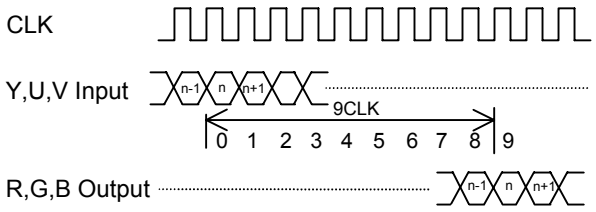
■ Input-and-output signal

Signal name	Polarity	I/O	Description
CLK	-	Input	Clock input
NRST	Low	Input	System reset input
Y[7:0]	-	Input	Y data input
U[7:0]	-	Input	U data input
V[7:0]	-	Input	V data input
RO[7:0]	-	Output	R data output
GO[7:0]	-	Output	G data output
BO[7:0]	-	Output	B data output

■ Block diagram



■ Time chart



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