# MS70203IP

## RGB to YUV Conversion IP module (Verilog HDL)

### ■ Outline

MS70203IP is IP module which changes RGB image data signal to YUV image data signal.

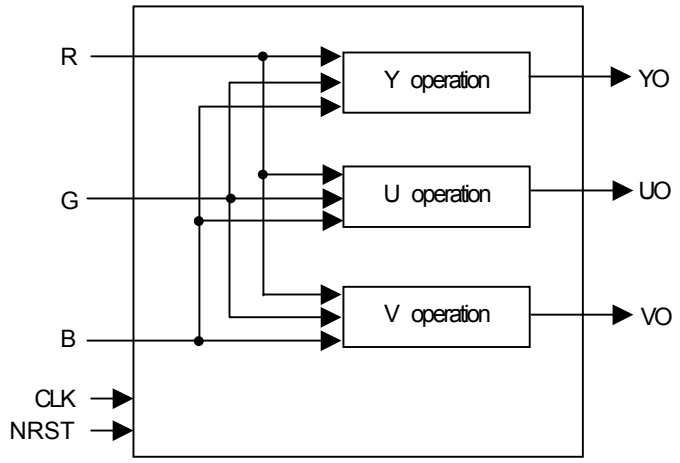
### ■ Feature

- Input and output data width 8 bits.
- High speed pipeline operation processing.
- Compatible with Conversion operation ITU-RBT-601.

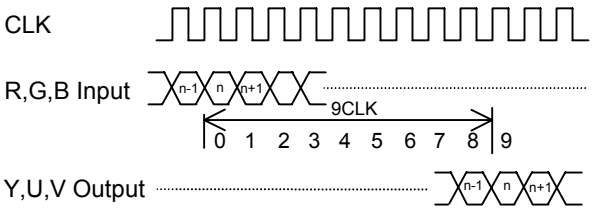
### ■ Input-and-output signal

| Signal name | Polarity | I/O | Description |
|---|---|---|---|
| CLK | - | Input | Clock input |
| NRST | Low | Input | System reset input |
| R[7:0] | - | Input | R data input |
| G[7:0] | - | Input | G data input |
| B[7:0] | - | Input | B data input |
| YO[7:0] | - | Output | Y data output |
| UO[7:0] | - | Output | U data output |
| VO[7:0] | - | Output | V data output |

### ■ Block diagram




### ■ Time chart

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